HOS Amplifiers

1. Biasing

A) Resistive Biasing

\[ I_D = k_n \cdot \frac{1}{2} \left[ V_{AS} - V_{TN} \right]^2 \]

\[ k_n = \mu_n \cdot C_{ox} \left( \frac{W}{L} \right) \]  \quad (1)

Furthermore

\[ I_D = \left| V_A - V_{AS} \right| \frac{1}{R_s} \]  \quad (2)

and

\[ V_A = V_{ON} \cdot \frac{R_s}{R_1 + R_s} \]  \quad (3)

Solving eq. (1) for \( V_{AS} \) yields

\[ V_{AS} = \sqrt{\frac{2I_D}{k_n}} + V_{TN} \]  \quad (1')

Finally, by inserting eq. (1') in (2), we obtain

\[ I_D = \left| V_A - V_{TN} - \sqrt{\frac{2I_D}{k_n}} \right| \frac{1}{R_s} \]  \quad (4)
Solving eq. (4) for $r_s$ yields:

$$
x_s = (V_G - V_tn) \frac{r_s}{2} - \sqrt{\frac{2}{k_n}}
$$

(5)

Using eq. (4) to calculate $I_D$ requires solving a quadratic equation with the argument $V_{D1}$.

The solution for $V_{D1}$ is:

$$
\frac{1}{\sqrt{I_D}} = \frac{1}{2k_n} \frac{1}{r_s} \left[ \sqrt{1 + (V_G - V_tn)2k_nr_s} - 1 \right]
$$

(6)

or

$$
I_D = \frac{1}{r_s} \left[ V_G - V_tn + \frac{1}{k_nr_s} \left( 1 - \sqrt{1 + (V_G - V_tn)2k_nr_s} \right) \right]
$$

(7)

The drain-source voltage can now be computed as:

$$
V_{DS} = V_{DN} - I_D (\bar{R}_D + r_s)
$$

(8)

**Numerical Example**

\begin{align*}
V_{DN} &= 5V \\ V_tn &= 0.7V \\ k_n &= 200 \mu A/V^2 \\
\bar{R}_D &= 250k \Omega \\ \bar{R}_S &= 270k \Omega & \Rightarrow & \left\{ V_G = 2.7V \right\} \\
\bar{R}_D &= 18k \Omega \\ \bar{R}_S &= 10k \Omega \\
I_D &= 10^{-4} \left[ 2 + \frac{1}{2} \left( 1 - \sqrt{1 + 5^2} \right) \right] [A] \\
I_D &= 100 \mu A \\
V_{DS} &= 2.2 V
\end{align*}
Biasing with Current Sources

**Idea:** By embedding the gain stage between 2 identical current sources, the gate voltage of the MOS amplifier becomes arbitrary (within practical limits).

**Concept**

\[ V_{DD} \]
\[ I_{DD} \]
\[ V_{G} \]
\[ I_{DD} \]
\[ M_{1} \]

**Practical Implementation**

\[ V_{DD} \]
\[ R_{P} \]
\[ M_{81} \]
\[ M_{82} \]
\[ M_{83} \]
\[ M_{84} \]

The 2 current sources are realized by establishing a reference current in an additional branch and mirroring this current onto the gain stage \((M_{1})\) by using 2 transistors \((M_{83} \& M_{84})\), which are identical to their counterparts \((M_{81} \& M_{82})\) in the reference branch.

\[ \rightarrow \] Current Mirror

**Note:** This biasing method only establishes the dc drain current \(I_{DD}\) of the gain stage. The drain-source voltage will depend on the actual output resistors of the MOS
devices in the gain stage, i.e., $T_{M31}$, $T_{M32}$ and $T_{M33}$.

The reference current $I_{ef}$ can be calculated as follows:

$$I_{ef} = \frac{1}{R_{ef}} \left[ V_{dd} + V_{asM32} - V_{asM33} \right] \quad (9)$$

where

$$V_{asM31} = V_{dd} - \sqrt{\frac{2 I_{ef}}{k_p}} \quad (10)$$

and

$$V_{asM32} = V_{dd} + \sqrt{\frac{2 I_{ef}}{k_n}} \quad (11)$$

**Note:** The threshold voltage $V_{th}$ of the $p$-channel device is negative!

Practically, eq. (9) is applied to solve for the reference resistor $R_{ef}$, since the designer selects the desired operating-point current $I_{ef}$ with regard to the specific application.

**Numerical Example**

<table>
<thead>
<tr>
<th>$V_{dd}$ = 5V</th>
<th>$V_{in}$ = 0.7V</th>
<th>$V_{th}$ = -0.7V</th>
<th>$k_p$ = 200μA/V$^2$</th>
<th>$k_n$ = 200μA/V$^2$</th>
<th>$I_{ef}$ = 100μA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{asM31}$ = -1.7V</td>
<td>$V_{asM32}$ = +1.7V</td>
<td>$R_{ef}$ = 16kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2. MOS Gain Stages

A) **Common-Source (CS) Amplifier**

2.1 **CS Amplifier with Resistor Biasing Circuit**

\[ V_{DD} \]
\[ \pi_1 \]
\[ \pi_0 \]
\[ C_i \]
\[ M_1 \]
\[ V_i \]
\[ \pi_2 \]
\[ \pi_3 \]
\[ C_s \]
\[ V_0 \]

**AC equivalent circuit (caps act as AC shorts)**

\[ V_i \]
\[ \pi_6 \]
\[ g_m V_i \]
\[ V_o \]
\[ \pi_0 \]
\[ \pi_7 \]

\[
\begin{align*}
\pi_G &= \pi_1 \parallel \pi_2 \\
g_m &= \sqrt{2I_D, K_i} \\
R_{o1} &= \frac{1}{g_m I_D}
\end{align*}
\]

**Input resistance:** \[ R_{in} = \pi_G \]

**Output resistance:** \[ R_{out} = R_{o1} \parallel \pi_0 \]

**Voltage gain:** \[ AV = \frac{V_o}{V_i} = -g_m R_{o1} \parallel \pi_0 \]
**Numerical Example**

\[ V_{DD} = 5V \quad V_{in} = 0.7V \quad \mu_i = 800\mu A/V^2 \quad \lambda = 0.025 \frac{V}{V} \]

\[ R_1 = 280k\Omega \quad R_2 = 220k\Omega \quad R_3 = 22k\Omega \quad R_5 = 10k\Omega \]

\[ I_{D_1} = 100\mu A \quad V_{DS} = 1.8V \quad V_{DS} = 1.2V \]

\[ f_m = 400\mu s \]

\[ r_{01} = 400k\Omega \]

\[ \pi_0 = 123.2k\Omega \]

**AC Performance**

\[ \pi_u = 123.2k\Omega \]

\[ R_{cut} = 20.85k\Omega \]

\[ AV = -8.74 \]

As demonstrated by this example, the CS amplifier using passive biasing yields relatively small voltage gain values. The gain could be increased slightly by increasing \( R_0 \) (e.g., \( R_0 = 30k\Omega \)). Unfortunately, increasing \( R_0 \) reduces the drain-source voltage (e.g., \( R_0 = 50k\Omega \), \( V_{DS} = 1.0V \)) and leaves little room for the output voltage swing. This dilemma can be overcome by employing an active biasing scheme.
2.2 CS Amplifier with current source biasing

Note: $V_s$ must comprise a dc component sufficiently large to keep $M_1$ in saturation

AC equivalent circuit (Caps act as AC Shorts)

\[ g_m = \sqrt{2I_d k_i} \]
\[ r_{oi} = \frac{1}{\lambda_i I_d} \quad r_{oi1} = \frac{1}{\lambda_{oi1} I_d} \]

Input resistance: \[ r_{in} = \infty \]
Output resistance: \[ r_{out} = r_{oi} \parallel r_{oi1} \]
Voltage gain:
\[ A_v = \frac{V_o}{V_i} = -g_m r_{oi} \parallel r_{oi1} \]
\[ A_v = -\frac{2k_i}{\lambda_i} \frac{1}{(\lambda_i + \lambda_{oi1})} \]
**Numerical Example**

\[ V_{DD} = 5V \quad V_{th} = 0.7V \quad h_i = 800 \mu A/V^2 \]
\[ I_{D1} = 100 \mu A \quad \lambda_i = 0.025 \frac{1}{V} \quad \lambda_{D1} = 0.025 \frac{1}{V} \]

\[ \begin{align*}
G_m & = 400 \mu S \\
T_{CI} & = 400 \Omega \\
T_{IS} & = 400 \Omega \\
V_{BS} & = 1.2V \\
V_{DS} & \approx 1.7V \\
\end{align*} \]

If all 3 MOS transistors are well matched.

**AC Performance**

\[ \begin{align*}
R_m & = \infty \\
R_{out} & = 200 \Omega \\
A_v & = -80 \\
\end{align*} \]

Replacing the passive load resistor \( R_o \) by an MOS current source (\( \rightarrow \) active load) allows the designer to realize a much larger voltage gain without sacrificing output swing. The price for this improvement is the need for multiple biasing transistors. However, this has little practical significance on an integrated circuit (IC), since a transistor requires less (silicon) area than a (large) resistor.
Special Case: Self-biased CMOS Inverter

Large Signal Response

No current flows if

\[ V_{in} < V_{th} \]

or

\[ V_{in} > V_{DD} - V_{th} \]

If \( M_1 \) and \( M_2 \) are well matched

\[
I_{D_{max}} = \frac{1}{2} I_P \left( \frac{1}{2} V_{DD} - V_{th} \right)^2
\]

\[
= \frac{1}{2} I_P \left( \frac{1}{2} V_{DD} - V_{th} \right)^2
\]
The self-biased CMOS Inverter

\[ +V_{DD} \]

\[ -V_{SS} \]

\[ \text{Vin} \rightarrow \text{M1} \rightarrow \text{M2} \rightarrow \text{Vout} \]

\[ CL \]

Linear gain

Assumption:

\[ \frac{1}{2} \mu_1 \left( \frac{W}{L} \right)_1 C_{ox} = \frac{1}{2} \mu_2 \left( \frac{W}{L} \right)_2 C_{ox} = k \]  

(1)

\[ A_v \equiv -\frac{4}{[V_{SS}-V_T][\lambda_1+\lambda_2]} \]  

(2)

where

\[ \lambda \equiv \frac{1}{L_{eff}} \sqrt{\frac{\varepsilon_S}{2 q N_{Sub} (\Phi_B+V_{DS})}} \]  

(3)

and

\[ L_{eff} \equiv L_{\text{Drawn}} - x_{LD} - \sqrt{\frac{2 \varepsilon_S (\Phi_B+V_{DS})}{q N_{Sub}}} \]  

(4)

Therefore

\[ A_v \propto L_{eff} \]  

(5)
Settling behavior

A) Linear

\[ V_{\text{out}}(t) = \Delta V A_v [1 - e^{-\frac{t}{\tau}}] \quad \text{for} \quad t \geq 0 \quad \text{and} \quad \Delta V \leq \frac{V_T}{|A_v|} \]  \tag{6}

where

\[ \tau \equiv \frac{C_L}{k} \frac{1}{(\lambda_1 + \lambda_2) [V_{SS} - V_T]^2} \]  \tag{7}

Consequently

\[ \tau \propto \frac{I_{\text{eff}}}{k} \propto L_{\text{eff}} \left( \frac{L}{W} \right) \]  \tag{8}

B) Nonlinear

\[ \mathcal{A}_1 \quad t_{\text{settl.}} \equiv \frac{C_L}{k} \frac{2 \sqrt{\Delta V(V_{SS} - V_T)^2 + (V_T - \Delta V)}}{2 \Delta V(V_{SS} - V_T)} \leq \Delta V \leq V_T \]  \tag{9}

\[ \mathcal{A}_2 \quad t_{\text{settl.}} \equiv \frac{C_L}{k} \frac{2 \sqrt{\Delta V(V_{SS} - V_T)^2 - (\Delta V - V_T)}}{2 V_{SS} \Delta V - \frac{1}{2} (\Delta V + V_T)^2} \quad V_T \leq \Delta V \leq (V_{SS} - V_T) \]  \tag{10}

\[ \mathcal{A}_3 \quad t_{\text{settl.}} \equiv \frac{C_L}{k} \frac{1}{\frac{1}{2} V_{SS} + (\Delta V - V_T)} \quad (V_{SS} - V_T) \leq \Delta V \leq V_{SS} \]  \tag{11}

Numerical Example (90% settling times according to SPICE)

<table>
<thead>
<tr>
<th>\Delta V [V]</th>
<th>t_{\text{settl.}} [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>10.4</td>
</tr>
<tr>
<td>0.3</td>
<td>7.6</td>
</tr>
<tr>
<td>0.4</td>
<td>6.0</td>
</tr>
<tr>
<td>0.6</td>
<td>4.4</td>
</tr>
<tr>
<td>0.9</td>
<td>3.1</td>
</tr>
<tr>
<td>1.2</td>
<td>2.5</td>
</tr>
<tr>
<td>1.6</td>
<td>2.0</td>
</tr>
<tr>
<td>2.0</td>
<td>1.6</td>
</tr>
<tr>
<td>2.5</td>
<td>1.4</td>
</tr>
</tbody>
</table>

\[ V_{DD} = V_{SS} = 2.5V \]
\[ V_T = 0.8V \]
\[ C_L = 400\text{fF} \]
\[ k = 100\mu A/V^2 \]
Static CMOS Logic Gates

Consider MOS device as ideal switch

NAND

Symbol

Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

$Q = \overline{A \cdot \overline{B}}$

Implementation

Switch which is closed while $A$ is high

CMOS Circuit
Symbol

\[ \begin{array}{c}
A \\
\overline{B}
\end{array} \rightarrow \begin{array}{c}
\overline{A} \\
A
\end{array} \rightarrow Q \]

Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Q</th>
</tr>
</thead>
<tbody>
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<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ Q = A + \overline{B} \]

Implementation

\[ \begin{array}{c}
\overline{B} \\
\overline{A} \\
A
\end{array} \rightarrow \begin{array}{c}
Q \\
\text{And}
\end{array} \]

CMOS Circuit

\[ \begin{array}{c}
\overline{B} \\
A
\end{array} \rightarrow \begin{array}{c}
Q \\
\text{And}
\end{array} \]
CMOS NOR Gate

CMOS NAND Gate

\[ +V_{DD} \]

\[ -V_{SS} \]

A

B

Q

A

B

Q