Traditional (static) CMOS Design

Basic Concept for Logic Gates

- PMOS
- NMOS
- Pull-up Logic
- Pull-down Logic
- Inputs

Pros
- Rail-to-Rail Output Swing
- No Static Power

Cons
- Stacked trans... slower response
- Complex gate structure for certain functions (e.g., XOR)

Note: Prop. delay $t_{pd}$ for gate with $n$ stacked transistors

$t_{pd}(n) \approx n \cdot t_{pd}(1)$
Basic Logic Gates

1. The MOS Inverter

Basic Configuration

\[ \text{Basic Configuration} \]

\[ \text{M1} \quad \text{M2} \]

\[ \text{V}_{\text{IN}} \quad \text{V}_{\text{OUT}} \]

a) Large Signal Response (DC transfer char.)

(for \( V_{\text{IN}} = V_{\text{IN}} \))

e.g. \( V_{\text{IN}} = 0 \)
The self-biased CMOS Inverter

![Circuit Diagram]

**Linear gain**

Assumption:

\[
\frac{1}{2} \mu_1 \left( \frac{W}{L} \right)_1 C_{ox} = \frac{1}{2} \mu_2 \left( \frac{W}{L} \right)_2 C_{ox} = k
\]  

(1)

\[
A_v \equiv - \frac{4}{[V_{SS} - V_T][\lambda_1 + \lambda_2]}
\]  

(2)

where

\[
\lambda \equiv \frac{1}{L_{eff}} \sqrt{\frac{\varepsilon_s}{2qN_{Sub}(\phi_B + V_{DS})}}
\]  

(3)

and

\[
L_{eff} \equiv L_{Drawn} - x_{LD} - \sqrt{\frac{2\varepsilon_s(\phi_B + V_{DS})}{qN_{Sub}}}
\]  

(4)

Therefore

\[
A_v \propto L_{eff}
\]  

(5)
Settling behavior

A) Linear

\[ V_{\text{out}}(t) = \Delta V A_v [1 - e^{-\frac{t}{\tau}}] \quad t \geq 0 \quad \text{and} \quad \Delta V \leq \frac{V_T}{|A_v|} \]  

(6)

where

\[ \tau \equiv \frac{C_L}{k} \frac{1}{(\lambda_1 + \lambda_2) [V_{SS} - V_T]^2} \]  

(7)

Consequently

\[ \tau \propto \frac{L_{\text{eff}}}{k} \propto L_{\text{eff}}\left(\frac{L}{W}\right) \]  

(8)

B) Nonlinear

\[ \text{A. I} \quad t_{\text{sett.}} \equiv \frac{C_L}{k} \frac{2 \sqrt{\Delta V(V_{SS} - V_T^2) + (V_T - \Delta V)}}{2 \Delta V(V_{SS} - V_T)} \quad \frac{V_T}{|A_v|} \leq \Delta V \leq V_T \]  

(9)

\[ \text{A. II} \quad t_{\text{sett.}} \equiv \frac{C_L}{k} \frac{2 \sqrt{\Delta V(V_{SS} - V_T^2) - (V_T - \Delta V)}}{2 V_{SS} \Delta V - \frac{1}{2}(\Delta V + V_T)^2} \quad V_T \leq \Delta V \leq (V_{SS} - V_T) \]  

(10)

\[ \text{A. III} \quad t_{\text{sett.}} \equiv \frac{C_L}{k} \frac{1}{\frac{1}{2} V_{SS} + (\Delta V - V_T)} \quad (V_{SS} - V_T) \leq \Delta V \leq V_{SS} \]  

(11)

Numerical Example (90% settling times according to SPICE)

<table>
<thead>
<tr>
<th>( \Delta V ) [V]</th>
<th>( t_{\text{sett.}} ) [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>10.4</td>
</tr>
<tr>
<td>0.3</td>
<td>7.6</td>
</tr>
<tr>
<td>0.4</td>
<td>6.0</td>
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</tr>
<tr>
<td>0.9</td>
<td>3.1</td>
</tr>
<tr>
<td>1.2</td>
<td>2.5</td>
</tr>
<tr>
<td>1.6</td>
<td>2.0</td>
</tr>
<tr>
<td>2.0</td>
<td>1.6</td>
</tr>
<tr>
<td>2.5</td>
<td>1.4</td>
</tr>
</tbody>
</table>
Inverter Trip-Point Voltage

At trip-point: \( V_{out} = \frac{1}{2} V_{dd} \)

\( I_p = I_n \)
both devices in saturation

Thus

\[
I_p = \beta_p \left[ V_{dd} - V_{trip} + V_{fp} \right]^2 \quad \beta_p = \frac{1}{2} \mu_p C_o \left( \frac{V}{2} \right)_p
\]

\[
I_n = \beta_n \left[ V_{trip} - V_{en} \right]^2 \quad \beta_n = \frac{1}{2} \mu_n C_o \left( \frac{V}{2} \right)_n
\]

\[ V_{dd} - V_{trip} + V_{fp} = \sqrt{\frac{\alpha_n}{\beta_p}} \left[ V_{trip} - V_{en} \right] \]

\[
V_{trip} = \frac{V_{dd} + V_{fp} + V_{en} \sqrt{\frac{\alpha_n}{\beta_p}}}{1 + \sqrt{\frac{\alpha_n}{\beta_p}}}
\]

Numerical Example:

\( V_{dd} = 7.5V \)
\( V_{en} = 0.7V \)
\( V_{fp} = -0.9V \)

Compute \( V_{trip} \) for a) \( \beta_n = \beta_p \)

b) \( \beta_n = 2\beta_p \)

c) \( \beta_n = 4\beta_p \)

Solutions:

a) \( V_{trip} = 1.55V \)

b) \( V_{trip} = 1.40V \)

c) \( V_{trip} = 1.27V \)
Basic Logic Gates Continued

NAND

Symbol

Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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<td>1</td>
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<td>1</td>
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<td>1</td>
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<td>0</td>
</tr>
</tbody>
</table>

\[ Q = \overline{A} \cdot \overline{B} \]

Implementation

Vdd

\[ \overline{A} \rightarrow \quad \overline{B} \rightarrow \quad 1 \quad \rightarrow \quad Q \quad \rightarrow \quad 1 \quad \rightarrow \quad \text{and} \]

where \[ \overline{A} \rightarrow \quad A \quad \rightarrow \quad \text{switch which is closed while } A \text{ is high} \]

CMOS Circuit

Vdd

\[ \overline{B} \rightarrow \quad \overline{A} \rightarrow \quad Q \quad \rightarrow \quad \text{and} \]
**NOR**

**Symbol**

\[
\begin{array}{c}
A \\
\overline{B} \\
\overline{A} \\
A
\end{array} 
\rightarrow Q
\]

**Truth Table**

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<thead>
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<th>A</th>
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</thead>
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</table>

\[Q = A + \overline{B}\]

**Implementation**

\[
\begin{array}{c}
\overline{B} \rightarrow \overline{A} \\
A \rightarrow \overline{A} \\
A \rightarrow B \\
\overline{B} \rightarrow Q
\end{array}
\]

**CMOS Circuit**

\[
\begin{array}{c}
\overline{B} \rightarrow Q \\
A \rightarrow \overline{A} \\
A \rightarrow B \\
\overline{B} \rightarrow Q
\end{array}
\]

**AND**
Symbol

\[ A \quad \overline{B} \quad \rightarrow \quad Q \]

Truth Table

<table>
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<th>\overline{B}</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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<tr>
<td>1</td>
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<td>0</td>
</tr>
</tbody>
</table>

\[ a = A \oplus \overline{B} \]

Composite Implementation

\[ A \oplus \overline{B} = \overline{A} \cdot \overline{B} + A \cdot \overline{B} = (A + \overline{B}) \cdot (\overline{A} + \overline{B}) \]

\[ = \overline{A} \cdot \overline{B} \]

\[ = (A + \overline{B}) + (\overline{A} + \overline{B}) \]

- 16 Trans.
- Rail-to-Rail
- Output Swing
- Comparatively slow

- 16 Trans.
- Rail-to-Rail
- Output Swing
- Comparatively slow
Complex Gate Implementation

**Pull-up Function**

\[ F_p = \overline{A \cdot \overline{B}} + A \cdot \overline{B} \]

**Pull-down Function**

\[ F_n = \overline{A \cdot \overline{B}} + A \cdot \overline{B} = A \cdot \overline{B} + \overline{A} \cdot B \]

- 8 Trans. if inputs are available in complementary form, otherwise 12 trans. are required
- Rail-to-Rail Output Swing
- comparatively fast
Static CMOS Power Dissipation

**Assumption:** Gate switches periodically from low to high with rail-to-rail swing. Switching period is $T_{sw}$.

**Model for switching gate**

\[
\begin{align*}
V_{out} & \quad R_a \quad C_L \\
\end{align*}
\]

**Assumption:**
\[
\begin{align*}
V_{out} &= V_{DD} \quad 0 \leq t < \frac{T}{2} \\
V_{out} &= 0 \quad \frac{T}{2} \leq t < T
\end{align*}
\]

\[HVLI: V_{out} = i(t)R_a + \frac{1}{C_L} \int i(t)dt \quad \frac{d}{dt}
\]

\[\therefore \quad \frac{d}{dt} i(t) = -\frac{1}{R_a C_L} i(t) \quad \text{i st order diff. eq.}
\]

**Solution**

\[i(t) = C_0 e^{-\frac{t}{R_a C_L}}
\]

**Initial Condition**

**Case A** \quad $V_{out} = V_{DD}$ (L $\rightarrow$ H transition)

\[i(0) = \frac{V_{DD}}{R_a} \quad \text{where} \quad R_a = R_p
\]

**Case B** \quad $V_{out} = 0$ (H $\rightarrow$ L transition)

\[i(0) = -\frac{V_{DD}}{R_a} \quad \text{where} \quad R_a = R_n
\]
**Power Dissipation**

\[ P = t^2 \mathcal{R} \]

\[ P_{L \rightarrow H} = \frac{V_{no}^2}{\pi \rho} e^{-\frac{2t}{\pi \rho \mathcal{R} C_L}} \quad 0 \leq t < \frac{T_{sw}}{2} \]

\[ P_{H \rightarrow L} = \frac{V_{no}^2}{\pi \rho} e^{-\frac{2t}{\pi \rho \mathcal{R} C_L}} \quad 0 \leq t < \frac{T_{sw}}{2} \]

**Average Power**

\[ P_{av} = \frac{1}{T} \int_0^T t^2 \mathcal{R} \, dt = \bar{P} \]

a) \[ \bar{P}_{L \rightarrow H} = \frac{2}{T_{sw}} \frac{V_{no}^2}{\pi \rho} \int_0^{T_{sw}} e^{-\frac{2t}{\pi \rho \mathcal{R} C_L}} \, dt \]

\[ = \frac{2}{T_{sw}} \frac{V_{no}^2}{\pi \rho} \frac{\pi \rho \mathcal{R} C_L}{2} (1 - e^{-\frac{T_{sw}}{\pi \rho \mathcal{R} C_L}}) \]

\[ \bar{P}_{L \rightarrow H} \approx \frac{2}{T_{sw}} \frac{V_{no}^2}{\pi \rho} \frac{\pi \rho \mathcal{R} C_L}{2} \]

b) \[ \bar{P}_{H \rightarrow L} = \frac{2}{T_{sw}} \frac{V_{no}^2}{\pi \rho} \int_0^{T_{sw}} e^{-\frac{2t}{\pi \rho \mathcal{R} C_L}} \, dt \]

\[ = \frac{2}{T_{sw}} \frac{V_{no}^2}{\pi \rho} \frac{\pi \rho \mathcal{R} C_L}{2} (1 - e^{-\frac{T_{sw}}{\pi \rho \mathcal{R} C_L}}) \]

\[ \bar{P}_{H \rightarrow L} \approx \frac{2}{T_{sw}} \frac{V_{no}^2}{\pi \rho} \frac{\pi \rho \mathcal{R} C_L}{2} \]
Conclusion: The average power dissipation of a static CMOS gate switched at a rate of $f_{sw}$ is independent of the gate topology and geometry.

\[ \bar{P} = \frac{1}{2} \bar{P}_{H \rightarrow L} + \frac{1}{2} \bar{P}_{L \rightarrow H} = V_{DD} C_L f_{sw} \]

Note: The above result neglects leakage currents and $V_{dd}$-to-$V_{ss}$ currents, which flow during the short time interval where both the pull-up and the pull-down path are active.

Leakage currents are very technology dependent ($V_T$ varies as processes are scaled) and change exponentially with temperature (each doubles approx. for every 11°C increase in temperature).

$V_{dd}$-to-$V_{ss}$ and currents can be minimized by keeping $f_{sw}$ and $f_{dd}$ short.

Thus

\[ \bar{I} = V_{DD} C_L f_{sw} + \bar{I}_{leak} + \bar{I}_{V_{dd}-V_{ss}} \]
Practical Question:
How wide do the power rails ($V_{PP}$ & $V_{AVG}$) have to be if they supply the current for $n$ gates?

Answer:
The current density should not exceed the critical density that causes electro-migration damage to the metal layer.
For aluminum rails, a safe density should be below $J_{crit} = 2 \text{ mA/\mu m}^2 \left(= 2 \times 10^9 \text{ A/m}^2\right)$

Numerical Example
A power rail drives 1,000 gates, which are switched at an average rate of 10 MHz. The average load per gate is 50F. How wide does the power rail have to be to keep the current density below 1 mA/\mu m² (assume an aluminum layer thickness of 1 \mu m), $V_{DD} = 5V$

Answers
\[
I = n \cdot V_{DD} \cdot C_{L} \cdot F_{SW} \cdot \frac{i}{W \cdot t}
\]
\[
W = n \cdot V_{DD} \cdot C_{L} \cdot F_{SW} \cdot \frac{i}{I \cdot t}
\]
$W_{min} = 1.5 \mu m$
**Pseudo-NMOS - A Design Alternative**

**Basic Configuration**

![N MOS Circuit Diagram](image)

Typical values for $V_{Vis}$ are $\frac{1}{2}V_{DD}$ or $V_{DD}$. Higher values for $V_{Vis}$ are preferred since they reduce the static power dissipation which occurs for low outputs.

**Example: XOR Gate**

\[ \text{XOR} = A \oplus B = A \bar{B} + \bar{A} B \]

Since NMOS NW pulls output down, its function is the inverse of the palse function. Thus \[ F_{\text{NMOS}} (A, B) = A \bar{B} + \bar{A} B \]

**Possible implementation**

![XOR Circuit Diagram](image)
Device sizing for pseudo-NMOS gates

Assumptions:
- Pull-down branch comprises 2 NMOS devices in series
- body effect is negligible
- logic low output voltage $V_L$ is much smaller than $(V_{DD} - V_{in})$

Objective: Keep $V_L$ lower than $V_{in}$ to prevent undesired turn on of NMOS devices in subsequent gates

Question: How do you size the NMOS gates and the pull-up PMOS gate to meet this objective?

Circuit Schematic

Since $V_L$ is small, we assume the 2 NMOS gates to be operated in the ohmic region. The PMOS gate, on the other hand, will be in the active region since its $V_{gs}$ will be close to $V_{DD}$. 

\[ V_{DD} \quad \text{assumption} \]
\[ V_L \quad \text{the 2 NMOS gates have identical geometry} \]
Equations:

\[ I_L = \mu_n \cos \left( \frac{V_x}{n} \right) \left[ (V_{sd} - V_x) V_x \right] \]  
\[ I_L = \mu_n \cos \left( \frac{V_x}{n} \right) \left[ (V_{sd} - V_x - V_m) (V_L - V_x) \right] \]  
\[ I_L = \mu_n \cos \left( \frac{V_x}{n} \right) \left[ (V_{sd} - V_x - V_m) \left( V_{in} - V_m \right) \right]^2 \]  

(1) + (2) \hspace{1cm} \left| V_L = \frac{V_x}{n} \frac{2V_{sd} - V_x - 2V_m}{V_{sd} - V_x - V_m} \right| \approx 2V_x \\
\left| V_x = \frac{1}{2} V_L \right| \\

(1) + (3) \hspace{1cm} \left| V_L = \frac{\mu_n \cos \left( \frac{V_x}{n} \right)}{2} \frac{\left[ (V_{sd} - V_x - 2V_m) \left( V_{sd} - V_x - V_m \right) \right]^2}{2V_{sd} - V_x - V_m} \right| \\
\left| V_L = \frac{\mu_n \left( \frac{V_x}{n} \right)}{2} \frac{\left[ (V_{sd} - V_x - 2V_m) \left( V_{sd} - V_x - V_m \right) \right]^2}{2V_{sd} - V_x - V_m} \right| \\

Numerical Example

\[ V_{sd} = 5 \text{ V} \quad \mu_n = 4.2 \times 10^{-2} \text{ m}^2 \text{ V}^{-1} \text{ s}^{-1} \]
\[ V_x = 1.65 \text{ V} \quad \mu_n = 1.6 \times 10^{-2} \text{ m}^2 \text{ V}^{-1} \text{ s}^{-1} \]
\[ V_m = 0.65 \text{ V} \]
\[ V_{in} = 0.55 \text{ V} \]
\[ \therefore V_L = \frac{0.14 \left( \frac{V_x}{n} \right)}{\left( \frac{V_x}{n} \right)} \text{ V} \]

If \( \left( \frac{V_x}{n} \right) \) is chosen equal to \( \left( \frac{V_x}{n} \right) \), then
\[ V_L \approx 140 \text{ mV} \]

This low value of \( V_L \) justifies our initial assumptions of NMOS device in ohmic region, pre-active and \( (V_{sd} - V_m) \gg V_L \).
Alternative implementation

\[
F_{NMOS}(A, I) = A \bar{I} + A \cdot I
\]

Pros
- Less complexity due to simplicity of pull-up logic

Cons
- Static power for all low outputs

7. Pre-charged logic

Idea: Maintain simplicity of pull-up logic but avoid static power of pseudo NMOS approach

- Clock pull-up devices (pulled logic to high)

Basic configuration

Note: The output is valid only during the active clock period
In order to avoid possible static power dissipation while the output is pre-charged, one can add a serial n-channel device to the NMOS driver network as shown below.

If the above gate configuration is followed by an inverter, one obtains the standard Domino Logic gate.

Pros
- No static power
- Good driving capability

Cons
- Susceptible to charge sharing in complex NMOS NW
- Output valid only during active clock phase
- Susceptible to leakage