I/O Considerations

Rule: All inputs to a chip and all (digital) outputs from a chip must be buffered.

In order to effectively drive large (e.g. 20 pF) external capacitive loads, the output buffers have to be very large. This can be achieved by cascading inverters with geometrically growing device cross-sections, e.g.

\[ S : S^3 : S^3 : S^4 \]

where \[ S^4 = \frac{C_L}{C_i} \]

Numerical Example

\[ C_L = 25 \text{ pF} \]
\[ C_i = 100 \text{ pF} \]

\[ s \approx 4 \]

Select inverter sizes: 4 : 16 : 64 : 250

n-channel: \[ 4x \frac{1}{2} \quad 6x \frac{1}{2} \quad 3x 8x \frac{1}{2} \quad 12x \frac{1}{2} \]

p-channel: \[ 5x \frac{1}{2} \quad 15x \frac{1}{2} \quad 5x 20x \frac{1}{2} \quad 12x 20x \frac{1}{2} \]
Minimize delay through inverter cascade

Basic Configuration

\[ \text{Propagation delay per stage:} \]
\[ \tau_{pd_i} = S \cdot \tau_{pd_0} \quad \text{where} \quad \tau_{pd_0} \text{ is minimum delay if inverter drives another inverter of identical size} \]

Maximum capacitor ratio

\[ R_0 = \frac{C_i \cdot S^{n+1}}{C_o \cdot S} = S^n \quad \text{so} \quad N = \frac{enR_0}{enS} \]

Propagation delay of cascade

\[ \tau_{pd} = N \cdot S \cdot \tau_{pd_0} = enR_0 \cdot \frac{S}{enS} \cdot \tau_{pd_0} \]

\[ \tau_{pd \min} \quad \text{set} \quad \frac{d\tau_{pd}}{ds} = 0 \quad \text{so} \quad \ln s - 1 = 0 \]

\[ s_{pd} = e \]

<table>
<thead>
<tr>
<th>( s )</th>
<th>( \frac{\text{units}}{s} )</th>
</tr>
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<tbody>
<tr>
<td>2</td>
<td>2.72</td>
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<tr>
<td>3</td>
<td>2.77</td>
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<tr>
<td>4</td>
<td>2.89</td>
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<tr>
<td>5</td>
<td>3.11</td>
</tr>
<tr>
<td>6</td>
<td>3.55</td>
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Tri-State Drivers (I-State Outputs)

Tri-state drivers are frequently used to access a common bus or to drive pads that can be configured either as inputs or outputs.

When using tri-state buffers (inverters) to access a common bus, special care has to be taken to control the various enable signals such that only one buffer writes to the bus at any given time.

Basic Tri-state Inverter
Basic Tri-state Buffer

The presented solutions are compact but possess limited driving capability due to the cascade of 2 transistors in both the pull-up and pull-down branch. If large capacitive loads have to be driven, the following solution is preferred.

\[
G_p = \overline{\text{In}} \cdot \overline{\text{En}}
\]

\[
G_n = \overline{\text{In}} \cdot \overline{\text{En}} \cdot \text{Tin} \cdot \overline{\text{En}}
\]

Required to drive large output transistors

<table>
<thead>
<tr>
<th>En</th>
<th>In</th>
<th>Gn</th>
<th>Gp</th>
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Tri-State CMOS Buffer
Tri-state CMOS Buffer

(V) : t(s)

v(in)

(V) : t(s)

v(en)

(V) : t(s)

v(out)

0.0  20n  40n  60n  80n

0.0  20n  40n  60n  80n
Input Protection Circuit
(Electro Static Discharge ESD)

Due to the thin gate oxide, MOS gates are particularly sensitive to voltage excursions on their gates. To prevent a fatal oxide punch through, all inputs to a chip must be protected with an ESD path.

Typical Input Protection Circuit

The diodes clamp the gate voltage to ground $V_d$ or $V_{dd} + V_d$, respectively, while the series resistor limits the current. Frequently, the 2 diodes are replaced by diode connected MOS transistors as shown below.
output pad with driver and ESD protection
Input Pad with ESD Circuit
Pad Frame 28 (1.5 mm x 1.5 mm)