Operational Amplifiers and Comparators

1. Overview

Op amp internal functions

Optional

Basic 2-Stage CMOS Opamp
Differential to Single-ended Conversion

Basic Configuration (p-channel load)

\[ V_{dd} \]

\[ V_{o1} \]
\[ V_{o2} \]
\[ I_1 \]
\[ I_2 \]

DC Symmetry: \( f_{m1} = f_{m2} \)

AC Differential mode

\[ I_1 = -I_2 \]

Linear equivalent Circuit (\( V_{dd} \approx Gnd \))

\[ V_{o1} = (I_1 - f_{m1}V_{o1})V_{o1} \quad (1) \]
\[ V_{o2} = (I_2 - f_{m2}V_{o2})V_{o2} \quad (2) \]
\[ I_1 = -I_2 \quad (3) \]

From (1)

\[ TL_1 = \left[ \frac{V_{o1}}{I_1} = \frac{V_{o1}}{I_1 - f_{m1}V_{o1}} \right] \]

\[ (1) + (2) \quad V_{o2} = (I_2 - I_1 \frac{f_{m2}V_{o1}}{I_1 + f_{m1}V_{o1}})V_{o2} \quad (4) \]

\[ (3) \times (4) \quad \frac{V_{o2}}{I_2} = TL_2 = (1 + \frac{f_{m2}V_{o1}}{I_1 + f_{m1}V_{o1}})V_{o2} \equiv 2V_{o2} \quad (5) \]

Diff. Gain:

\[ V_{o1dm} = -\frac{1}{2} V_{dm} g_{min} TL_1 \equiv -\frac{1}{2} V_{dm} \frac{g_{min}}{f_{m1}} \]
\[ V_{o2dm} = \frac{1}{2} V_{dm} g_{min} TL_2 \equiv V_{dm} g_{min} \]
Note: Under common mode (CM) input conditions, eq. (5) has to be replaced by
\[ V_{cm} = V_{cm}^{'} = \frac{1}{2} \frac{V_{cm}}{R_{ss}} \] (7')

where \( R_{ss} \) denotes the output resistance of the load current source \( I_{ss} \).

Equation (5) then changes to
\[ \frac{V_{o2}}{V_{o2}} = V_{o2} = (1 - \frac{g_{m2} R_{o2}}{1 + g_{m1} R_{o1}}) V_{o2} = \frac{1}{g_{m1}} \] (5')

Therefore
\[ V_{o2} = \frac{1}{2} V_{o2} \frac{V_{o2}}{R_{ss}} = \frac{1}{2} V_{o2} \frac{g_{m1} R_{ss}}{1} \]
\[ V_{o2} = \frac{1}{2} V_{o2} \frac{V_{o2}}{R_{ss}} = \frac{1}{2} V_{o2} \frac{g_{m1} R_{ss}}{1} \]

Summary

| Diff. Gain | \( A_{dm} = g_{m1} I_{o2} \) |
| CM Gain | \( A_{cm} = \frac{I}{2} \frac{1}{g_{m1} R_{ss}} \) |
| CMRR | \( \frac{A_{dm}}{A_{cm}} = 2 \frac{g_{m1} I_{o2}}{g_{m1} R_{ss}} \) |
2. Design for DC

A) DC BIASING \((V_i = 0)\)

\[ \frac{i}{2} I_{OFF} = \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right) \left[ V_{GS1} - V_T \right]^2 \]

\[ V_{GS1} = -V_S \quad (V_i = 0) \]

\[ \Rightarrow V_S = -\left[ V_{TH} + \sqrt{\frac{2I_{OFF}}{\mu C_{ox} \left( \frac{W}{L} \right)}} \right] \]

\[ \frac{i}{2} I_{INFH} = \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right) \left[ -V_{GS2} + V_T \right]^2 \]

\[ V_{GS2} = -(V_{DD} - V_T) \]

\[ \Rightarrow V_0 = V_{DD} - \left[ -V_T + \sqrt{\frac{I_{INFH}}{\mu C_{ox} \left( \frac{W}{L} \right)}} \right] \]

Note: To achieve a large input common mode range, keep \(V_S\) close to zero and \(V_0\) close to \(V_{DD}\). To choose a small value for \(I_{OFF}\), as we shall see, this also yields a maximum gain. The price for these improvements is a reduction in the amplifier speed.
3) Systematic Offset Voltage

To obtain zero systematic offset, \( V_0 \bigg| = 0 \). This implies that \( I_3 = I_4 = \frac{1}{2} I_{\text{diff}} \).

Since \( M_3, M_4 \), and \( M_6 \) are all p-type transistors with the same \( V_{G5} \), we can write:

\[
\frac{I_{\text{diff}}}{I_{\text{out}}} = \frac{2(\frac{W}{L})_3}{(\frac{W}{L})_6} = \frac{2(\frac{W}{L})_4}{(\frac{W}{L})_6} \quad (1)
\]

Similar arguments applied to \( M_7 \) and \( M_9 \) yields:

\[
\frac{I_{\text{diff}}}{I_{\text{out}}} = \frac{W}{L} \quad (2)
\]

Thus, to achieve zero systematic offset, we must satisfy the following equation:

\[
\frac{2(\frac{W}{L})_3}{(\frac{W}{L})_6} = \frac{2(\frac{W}{L})_4}{(\frac{W}{L})_6} = \frac{W}{L} \quad (3)
\]
C) Random Offset Voltage

If offsets in $V_t$ and $(\frac{W}{L})$ in the differential input stage only are considered, a straightforward analysis gives:

$$V_{os} = V_t + \frac{1}{2} \sum \frac{g_{m3 - 4} \cdot (W/L)_{1 - 2}}{g_{m1 - 2}}$$

Mismatch of loads reduced by $g_{m3}/g_{m1}$

- Operate input stage at low bias to minimize offset
- Realize small ratio of $g_{m3}/g_{m1}$

3. Design for AC

A) Compensation

$$A = A_1 \cdot A_2$$

$C_1$, $C_2$: Parasitic Capacitances
Gain Phase Plot

- Pole $p$, due to $C_1$
- Pole $p_2$, due to $C_2$

Zero phase margin

Operate in feedback configuration:
- $180^\circ$ phase shift due to neg. feedback
- $180^\circ$ phase shift due to parasitic poles
  $\Rightarrow$ total phase shift: $360^\circ$ i.e. neg. feedback becomes positive
  $\Rightarrow$ instability

$\Rightarrow$ Additional phase compensation required
Pole Splitting Compensation

$C_c$ pushes pole 1 lower in frequency due to Miller multiplication. It pushes pole 2 higher in frequency.

At $|A_1| > 1$, $\phi = -\frac{3}{4} \pi$

$\Rightarrow$ Phase margin $\approx \frac{1}{4} \phi \approx 45^\circ$
Quantitative Description

Small Signal model of Opamp

\[ V_i - g_m V_i' = \frac{g_m}{g_m + g_{o2}} V_i - \frac{g_{o2}}{g_m + g_{o2}} V_o \]

\[ V_i' = g_m + g_{o2} \]

\[ V_o = \frac{g_m (g_m - g_{o2}) (1 + \frac{g_{o2}}{g_m})}{g_m + g_{o2} + g_{o1} + g_{o2} + g_{o3} + g_{o4}} \]

Source Follower Node: without \( C_c \) (\( C_c = 0 \))

\[ V_o = \frac{g_m g_{o2}}{g_{o1} g_{o2} + (1 + \frac{g_{o2}}{g_m}) (g_m + g_{o2} + g_{o3} + g_{o4})} \]

\[ V_o = \frac{g_m}{g_{o1} g_{o2} + (1 + \frac{g_{o2}}{g_m}) (g_m + g_{o2} + g_{o3} + g_{o4})} \]

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Right Half plane zero addition increases phase margin.

Solution: Zero must be shifted over to left half plane.

- With a Source Follower in the feedback path:
  \[ \tilde{z}_1 \rightarrow \infty \]

  - Eliminates RHP zero.
  - Costs:
    - Area
    - Power

- With a resistor \( R_z \) in the feedback path:
  \[ \tilde{z}_1 = -\frac{g_m}{C_c(g_m R_z - 1)} \]

  - If \( g_m R_z = 1 \) zero cancelled
  - If \( g_m R_z > 1 \) LHP zero

  - Conserves no additional power
  - Requires little additional area
2-Stage CMOS Amplifier
Two-stage Differential Amplifier

By replacing all transistors by their linear equivalent circuits and using first-order analysis techniques, the amplifier differential gain $A_d$ and the common mode rejection ratio CMRR turn out to be:

$$A_d = \frac{g_{m1}r'_{03} g_{m6}r'_{06}(1 + sC_c[r_{05} - \frac{1}{g_{m6}}])}{1 + s[C_c r'_{03} g_{m6}r'_{06} + C_L r'_{06}] + s^2 C_c C_L r'_{03} r'_{06}}$$

$$CMRR = 2g_{1}r_{08} g_{m5} r'_{03}$$

where $g_1 = g_{m1} + g_{m5}$ $r'_{03} = \frac{r_{na} r_{oa}}{r_{oa} + r_{03}}$ $r'_{06} = \frac{r_{na} r_{oa}}{r_{oa} + r_{07}}$

The two parameters $g_m$ and $g_{bm}$ denote the transistor gate-source transconductance and body-source (or backgate) transconductance, respectively.

The two poles and the zero that are present in the gain expression are approximately located at:

$$\omega_z = -\frac{g_{m6}}{C_c [g_{m6} r_{05} - 1]}$$

$$\omega_{p1} = -\frac{1}{C_c r'_{03} g_{m6} r'_{06}}$$

$$\omega_{p2} = -\frac{g_{m6}}{C_L}$$

Note that in order to guarantee a left half-plane zero, the product $g_{m6} r_{05}$ has to be greater than 1.

Most often, the nondominant second pole and the zero of the amplifier are kept equal to or greater than the unity-gain frequency GB. The frequency response can then be modeled by a first-order lowpass circuit. The unity-gain frequency is then approximately equal to:

$$GB = |A_d \omega_{p1}| = \frac{g_{m1}}{C_c}$$
Amplifier in Feedback Configuration

\[ V_0 = (V_i - \frac{V_o}{k}) - A \quad k \geq 1 \]

\[ \left| \frac{V_o}{V_i} = \frac{A}{1 + \frac{A}{k}} \right| \]

\[ A(s) = \frac{A_0}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})(1 + \frac{s}{p_3})} \quad p_1, p_2, p_3 \text{ are real poles} \]

- Is the circuit stable for all possible values of \( k \) ?
- Find poles of closed loop system as a function of feedback parameter \( k \)

\[ \left| \frac{V_o(s)}{V_i(s)} = \frac{A_0}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})(1 + \frac{s}{p_3}) + \frac{A_0}{k}} \right| \]

- Find Root Locus plot for the 3 poles as a function of \( k \)

Characteristic equation of closed-loop system

\[ D(s) = 1 + \frac{A}{A_0} \left( \frac{s}{p_1} \right) \left( \frac{s}{p_2} \right) \left( \frac{s}{p_3} \right) \quad 1 \leq k < A_0 \]

\[ D(s) = 1 + \mu \cdot e(s) \quad \mu = \frac{A}{A_0} \quad \frac{1}{A_0} \leq \mu < 1 \]
Root Locus Plot for 1 rep. real poles in open-loop

Note: No. for stability

\( k = 1 \) (unity gain)

Conclusion:
Depending on the initial position of the open-loop poles, the closed-loop system can become unstable as \( k \) approaches 1.

Note:
If initial poles are closely spaced, the system is very likely to become unstable in a closed-loop configuration.

Solution: Split poles apart

\[ p_2 \approx \lambda \cdot p_1, \quad p_3 > p_2 \]
### Opamp Stability Analysis

#### Pole/zero locations as a function of Phase Compensation Circuitry

<table>
<thead>
<tr>
<th>pole/zero</th>
<th>uncomp.</th>
<th>$C_c + R_c$</th>
<th>Source Follower</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_z$</td>
<td>$\infty$</td>
<td>$-\frac{g_{m2}}{C_c [g_{m2} R_c - 1]}$</td>
<td>$-\frac{g_{m5}}{C_c}$</td>
</tr>
<tr>
<td>$\omega_{p1}$</td>
<td>$-\frac{1}{r_0 C_1}$</td>
<td>$-\frac{1}{r_0 C_s g_{m2} r_2}$</td>
<td>$-\frac{1}{r_0 C_s g_{m2} r_2}$</td>
</tr>
<tr>
<td>$\omega_{p2}$</td>
<td>$-\frac{1}{r_2 C_2}$</td>
<td>$-\frac{g_{m2}}{C_2 \left[ 1 + \frac{C_1}{C_0} + \frac{C_2}{C_1} \right]}$</td>
<td>$-\frac{g_{m2}}{C_2 \left[ 1 + \frac{C_1}{C_0} + \frac{C_2}{C_1} \right]}$</td>
</tr>
</tbody>
</table>

#### Numerical Example

<table>
<thead>
<tr>
<th>$g_{m2} = 5.00 \mu S$</th>
<th>$g_{m5} = 100 \mu S$</th>
<th>$R_c = 12 \text{k}\Omega$</th>
<th>$r_0 = 500 \text{k}\Omega$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r_0 = 260 \text{k}\Omega$</td>
<td>$C_1 = 200 \mu F$</td>
<td>$C_2 = 5 \mu F$</td>
<td>$C_s = 2 \mu F$</td>
</tr>
</tbody>
</table>

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<tbody>
<tr>
<td>$\omega_z$</td>
<td>$\infty$</td>
<td>$-5 \times 10^6$</td>
<td>$-5 \times 10^6$</td>
</tr>
<tr>
<td>$\omega_{p1}$</td>
<td>$-1 \times 10^6$</td>
<td>$-1 \times 10^6$</td>
<td>$-1 \times 10^5$</td>
</tr>
<tr>
<td>$\omega_{p2}$</td>
<td>$-1.0 \times 10^6$</td>
<td>$-8.7 \times 10^6$</td>
<td>$-8.7 \times 10^6$</td>
</tr>
<tr>
<td>$\omega_{p3}$</td>
<td>$\infty$</td>
<td>$-4 \times 10^6$</td>
<td>$-5 \times 10^6$</td>
</tr>
</tbody>
</table>
4. **Slew Rate**

\[
\begin{align*}
\text{Slew Rate limit:} \\
SR &= \frac{dV_{out}}{dt} \\
&= \min \left\{ \frac{I_{\text{max}}}{C_c}, \frac{I_{2 \text{max}}}{(C_c + C_L)} \right\} \\
\text{Note: } I_{\text{max}} &= I_{\text{diff}} \\
&I_{2\text{max}} = I_{\text{out}} \quad \text{(for class A output stage)}
\end{align*}
\]

If \(SR_1 = SR_2\) \(: \frac{I_{\text{diff}}}{C_c} = \frac{I_{\text{out}}}{C_c + C_L}\) or \(I_{\text{out}} = I_{\text{diff}}(1 + \frac{C_L}{C_c})\)

If second pole of amplifier is at the unity-gain frequency, then \(|Q_{13}| \approx \frac{2 \omega_{\text{in}}}{C_c}|\)

Furthermore, if \(SR = SR_2 = \frac{I_{\text{diff}}}{C_c}\) then \(SR = \frac{Q_{13}}{\omega_{\text{in}}} \frac{I_{\text{diff}}}{\frac{C_L}{C_c}}\)

Since \(G_{13} = \sqrt{\mu \cdot C_{ox}(\frac{L}{W}) \cdot \frac{1}{2} \cdot I_{\text{diff}} \cdot 2}\)

We obtain \(SR \approx Q_{13} \sqrt{\frac{I_{\text{diff}}}{\mu \cdot C_{ox}(\frac{L}{W})}}\)
Performance Criteria and Design Guidelines

1. Gain
   - Low bias current
   - Long devices $\rightarrow$ high $V_o$
   - Wide devices $\rightarrow$ high $f_m$
   - Cascade configuration

2. Bandwidth ($\frac{f_m}{C}$)
   - High bias current
   - Short channel

3. Slew Rate
   - High bias current

4. Offset Voltage
   - Large devices
   - Low bias current $\rightarrow$ small $V_{off}$

5. Noise
   - Large devices $\rightarrow$ less $1/f$ noise
   - High bias $\rightarrow$ high $f_m$

Good Design = Good Compromise among Conflicting Criteria
OpAmp Performance Evaluation

Test Circuit Set-up for Spice
0.5 µm CMOS OPAMPS
Low-Voltage Amplifiers

In order to keep the signal-to-offset and signal-to-noise ratio as large as possible, circuits must be designed which have rail-to-rail input and output voltage swing.

A) Input stage with Rail-to-Rail Swing

Basic configuration

![Circuit Diagram]

Problem: Transconductance of input stage varies as Vin is changed
Solution: Keep total diff. input current constant

Resulting input transconductance

Comment: This solution works fine if the input stages are operated in weak inversion where the transconductance is proportional to the bias current. For the more typical case, however, where the input stages are operated in strong inversion (i.e. saturation), a 40% decrease in current since

\[ g_m \propto \left[ \frac{1}{\sqrt{I_{ox} x}} + \sqrt{I_{ox} (1-x)} \right] \]

so that

where \( Max \left[ \frac{1}{\sqrt{I_{ox} x}} + \sqrt{I_{ox} (1-x)} \right] = 1.41 \sqrt{I_{ox}} \)
Improved Solution

Resulting Transconducance (for saturation)
CMOS Amplifier with Rail-to-Rail Common-Mode Input Range

Core Amplifier Circuit

Bias Circuitry
High Gain CMOS Opamp with Cascode Input Stage

Version 1 with n-channel Input Pair

+Vdd

mb1

m7

m10&11

m8

m13

Cc

3pF

Out

Cl

10pF

-Vss

mb2

-\text{In}

mb3

2x120/4

2x120/4

2x120/4

2x120/4

m1

m2

m3

m4

m5

m6

m9

m12

15/4

5/4

60/4

2x100/4

2x100/4

2x100/4

2x100/4

2x100/4

2x100/4

25/4

2x120/4

2x120/4

2x120/4

2x120/4
CMOS Amplifier with Cascode Differential Stage

Transfer Characteristic

(V) : VOLTS(V)

v(out)

(VOLTS(V))

Amplitude Response (CL=10pF)

(Mag(V)) : f(Hz)

vm(out)

1meg

100k

10k

1k

100

10

1

0.1

(10.0, 570900.0)

(32.74meg, 1.007)

Phase Response (CL=10pF)

(Phase(deg)) : f(Hz)

vp(out)

0.0

-25.0

-50.0

-75.0

-100.0

-125.0

-150.0

-175.0

10.0

100.0

1.0k

10.0k

1meg

10meg

100meg

(32.7meg, -129.6)
High Gain CMOS Opamp with Cascode Input Stage

Version 2 with p-channel Input Pair
CMOS Transconductance Amplifier
CMOS Push-Pull Amplifier with high Current Driving Capability
Folded Cascode Transconductance Amplifier with passive Common Mode Feedback
Folded Cascode Fully-Differential Transconductance Amplifier with active CMF
COMPARATORS

A. Definition and Features

B. Requirements

1. HIGH GAIN 10K  Alternative: Employ positive feedback
2. LOW OFFSET VOLTAGE
3. COMMON MODE REJECTION ≈ 40dB
4. FAST RESPONSE < 1μsec
5. LOW POWER; SMALL AREA
6. STROBE
Sampled-Data Comparator  Version 1

Clocking Scheme
Offset compensated Sampled Data Comparator

Output

Inverter2

Inverter3

Input

Clock (400MHz)

Power Dissipation

(TPOWRD) : t(s)

(TPOWRD(power))
Sampled-Data Comparator  Version 2

Clocking Scheme
CMOS Comparator with Hysteresis  Version 4

\[ V_{\text{hyst}} = \sqrt{\frac{2 I_f}{\mu C_{ox} (W/L)_{th}}} \left[ \sqrt{K} - 1 \right] \]

Where \( K = \frac{(W/L)_1}{(W/L)_5} \)  \( K > 1 \)

\[ V_{\text{hyst}} \approx |V_{\text{eff}_1} - V_{\text{eff}_2}| @ \text{comp point} \]

Positive transition: \( I_1 = I_t \quad I_2 = I_0 = K \cdot I_t \quad I_3 = I_t + I_2 = I_3 \) (1st)

(\( M_4 \) and all off)

\[ V_{\text{eff}_1} = \sqrt{\frac{V_f}{(W/L)_1 \mu C_{ox} (L/W)_1}} \]

\[ V_{\text{eff}_2} = \sqrt{\frac{a I_t \cdot K}{(W/L)_5 \mu C_{ox} (L/W)_5}} \]
Comparator with Hysteresis

Res. trip point:

\[ i_o = \frac{(W/L)_o}{(W/L)_s} \quad i_s = i_2 \]

\[ i_s = i_1 + i_2 = i_1 + i_2 \]

\[ V_{\text{hyst}} = |V_{\text{eff1}} - V_{\text{eff2}}| \]
Latched CMOS Comparator
high-speed CMOS comparator

Power (5V Supply)

Sampled Output

100 MHz Sampling Clock

Intermediate Latch

Differential Input
high-speed cmos comparator

Power (5V Supply)

(TPOWRD) : t(s)

1TPOWRD(power)

Sampled Output

(V) : t(s)

v(out)

100 MHz Sampling Clock

(V) : t(s)

v(ckp)

Intermediate Latch

(V) : t(s)

v(o3)

Differential Input (25 MHz Sine)

(V) : t(s)

v(vin,vref)

t(s)
high-speed CMOS comparator with 2 differential input pairs

(V) : t(s)
v(vin,vin)

(V) : t(s)
v(o4)

(V) : t(s)
v(o3)

(V) : t(s)
v(nclk)

(V) : t(s)
v(out)