1. Basic Circuit

$V_{IN}$ $\rightarrow V_{G}$ $\rightarrow V_{OUT}$ $\rightarrow C_L$

$V_{H}$ $\rightarrow V_{L}$ $\rightarrow \text{Sample}$ $\rightarrow \text{Hold}$

acquisition time \[ T = \frac{1}{\tau_{ON}} \cdot C_L \]

\[ \tau_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_T)} \]

for small $V_{DS}$

Nonideal effects

A) Slow Case

assumptions:

$V_{IN} < (V_{H} - V_T)$

Switch turnoff
\[ V_{IN} C_L + (V_{IN} - V_{ch} + V_T) C_{OL} = (V_{IN} - \Delta V) C_L + (V_{IN} - \Delta V - V_L) C_{OL} \]

Charge at turn off

\[ -V_T C_{OL} = (V_{IN} - V_L) C_{OL} - \Delta V (C_L + C_{OL}) \]

\[ \Delta V = \frac{(V_{IN} + V_T - V_L)}{(C_L + C_{OL})} \]

\[ V_{OUT} = V_x = V_{IN} - \Delta V = \left( V_{IN} \frac{C_L}{C_{OL}} - V_T + V_L \right) \frac{C_{OL}}{(C_L + C_{OL})} \]

Gain Error: \[ E_s = -\frac{C_{OL}}{(C_L + C_{OL})} \]

Offset Error: \[ V_{OS} = -(V_T - V_L) \frac{C_{OL}}{(C_L + C_{OL})} \]

\[ (C_L \gg C_{OL}) \]

B) Fast Case

\[ V_g \]

\[ \frac{1}{2} Q_{ch} \leftarrow \text{Col} \rightarrow \frac{1}{2} Q_{ch} \]

\[ Q_{ch} = \frac{1}{2} W L C_{OX} (V_{OS} - V_T) = \frac{1}{2} W L C_{OX} (V_H - V_{IN} - V_T) \]

Charge balance:

\[ (V_{IN} - V_H) C_{OL} + V_{IN} C_L = \frac{1}{2} Q_{ch} + (V_{IN} - \Delta V - V_L) C_{OL} + (V_{IN} - \Delta V) C_L \]

Charge at turn off

\[ -(V_H - \Delta V) C_{OL} = \frac{1}{2} Q_{ch} - V_L C_{OL} - \Delta V C_L \]

\[ -(V_H - V_L) C_{OL} - \frac{1}{2} Q_{ch} = -\Delta V (C_L + C_{OL}) \]
\[ \Delta V = (V_H - V_L) \frac{C_{OL}}{(C_L + C_{OL})} + \frac{1}{2} W L (V_H - V_L - V_f) \frac{C_{OX}}{(C_L + C_{OX})} \]

\[ V_{OUT} = V_H - \Delta V = V_H (1 + \frac{1}{2} \frac{W L C_{OX}}{C_L + C_{OX}}) - (V_H - V_f) \frac{C_{OL}}{C_L + C_{OL}} - (V_H - V_f)^2 \frac{W L C_{OX}}{C_L + C_{OX}} \]

Gain Error:
\[ E_F = \frac{1}{2} \frac{W L C_{OX}}{(C_L + C_{OX})} \]

Offset Error:
\[ V_{OS_F} = - (V_H - V_L) \frac{C_{OL}}{C_L + C_{OL}} - (V_H - V_f)^2 \frac{W L C_{OX}}{C_L + C_{OX}} \]

**Numerical Example:**

\[ V_f = 1V; \quad V_H = 2.5V; \quad V_L = -2.5V \]

\[ C_L = 250fF; \quad L = 0.5\mu m; \quad W = 1\mu m \]

\[ L_D = 14nm \Rightarrow C_{OX} \approx 2.5 \frac{EF}{\mu m^2} \]

Overlap Cap:
\[ C_{OL} \approx W \cdot L_D \cdot C_{OX} \]

\[ L_D = 0.05\mu m \Rightarrow C_{OL} \approx 0.13fF \]

**Resulting Errors:**

**Slow Case:**
\[ E_S = -5.2 \times 10^{-4} \]
\[ V_{OS_S} = -0.5mV \]

**Fast Case:**
\[ E_F = 2.5 \times 10^{-2} \]
\[ V_{OS_F} = -6.4mV \]
Switched–Capacitor Sample and Hold

Track Phase (n–channel switching transistor is on)

\[ V_{g}=V_{dd} \]

\[ V_{o} = \text{Vin} \]

\[ Q_{ch} = C_{ch} (V_{dd} - V_{t}) \]

Assumption: \( \text{Vin} < V_{dd} - V_{t} \)

\[ V_{ot} = \text{Vin} \]

\[ Q_{ot} = V_{ot} \frac{C_{h}}{C_{h} + C_{o}} \]

\[ Q_{ch} = C_{ch} (V_{dd} - V_{t}) \]

where \( C_{ch} = W \frac{L}{t_{ox}} = W \frac{L}{C_{ox}} \)

Hold Phase (n–channel switching transistor is off)

\[ V_{g}=0 \]

\[ V_{o} = \text{Voh} \]

Assumption: \( V_{g} \) switches fast

\[ Q_{ch} = 0 \]

\[ Q_{oh} = V_{oh} (C_{h} + C_{o}) \]

Charge Conservation (Qot=Qoh)

\[ V_{oh} = \text{Vin} \left( \frac{C_{h} + C_{o} + C_{ch}/2}{C_{h} + C_{o}} \right) - V_{dd} \left( \frac{C_{o} + C_{ch}/2}{C_{h} + C_{o}} \right) + V_{t} \left( \frac{C_{ch}/2}{C_{h} + C_{o}} \right) \]

Gain Error:

\[ E_{g} = \frac{C_{ch}/2}{C_{h} + C_{o}} \]

Offset Error

\[ V_{os} = \frac{V_{t} (C_{ch}/2 - V_{dd} (C_{o} + C_{ch}/2))}{C_{h} + C_{o}} \]

where

\[ V_{o} = V_{o0} + \sqrt{ \frac{2q_{0}}{\sqrt{2q_{0}}}} \left( \frac{C_{ch}/2 - V_{dd} (C_{o} + C_{ch}/2)}{C_{h} + C_{o}} \right) \]
Charging and Discharging Hold Capacitor

Assumptions:

1. Switch is single n-channel transistor
2. \( V_{\text{in}} < V_{\text{DD}} - V_t \)
3. \( V_{\text{GG}} = V_{\text{DD}} \), \( V_{\text{GL}} = 0 \)

A) Charging Capacitor \((0 < V_{\text{in}} < V_{\text{DD}} - V_t)\)

\[
\begin{align*}
\dot{I}_{\text{switch}} &= \beta \left[ (V_{\text{DD}} - V_t)(V_{\text{in}} - V_0) - \frac{1}{2} (V_{\text{in}}^2 - V_0^2) \right] \\
T_{\text{on}} &= \frac{1}{\beta \left[ V_{\text{DD}} - V_t - V_0 \right]} & V_0 \leq V_{\text{in}}
\end{align*}
\]

where \( \beta = \frac{\mu}{L} C_{\text{ox}} \)

and \( V_t = V_{\text{DD}} + \sqrt{2 \Phi_F + V_{\text{DD}} - \sqrt{2 \Phi_F}} \)

Note: \( V_{\text{mmin}} = V_{\text{DD}} - V_t = V_{\text{in max}} \)

B) Discharging Capacitor \((V_{\text{in}} = 0)\)

\[
\begin{align*}
\dot{I}_{\text{switch}} &= \beta \left[ (V_{\text{DD}} - V_t) V_0 - \frac{1}{2} V_0^2 \right] \\
T_{\text{on}} &= \frac{1}{\beta \left[ V_{\text{DD}} - V_t - V_0 \right]} \\
\end{align*}
\]

Time constant: \( T = T_{\text{on}} C_h = \frac{C_h}{\beta \left[ V_{\text{DD}} - V_t - V_0 \right]} \)

\( \tau \propto \frac{1}{w \mu C_{\text{ox}}} \)

* Always use minimum channel length for switching device.
\[ V = 5 \alpha \]

\[ I_D = I_0 \]

\[ I_{D_{\text{Max}}} = \beta \left[ (V_{DD} - V_t) V_{in} - \frac{1}{2} V_{in}^2 \right] \]

\[ \beta = \frac{W}{L} \mu_C \]

\[ \tan \min = \frac{1}{\beta [V_{DD} - V_t]} \]

\[ \tan \max = \frac{1}{\beta [V_{DD} - V_t - V_{in}]} \]

**Notes:**
- \( V_t \) changes with bias, i.e. \( V_{in} \)
- \( \beta = \frac{W}{L} \mu_C \)

**Numerical Example:**
- \( V_{DD} = 5V \), \( V_t = 1V \) (body effect)
- \( \beta = 10^{-4} \text{A}^2/V \)
- \( V_{in} = 2V \)
- \[ I_{D_{\text{Max}}} = 0.6 \text{mA} \]
- \[ \tan \min = 2.5 \text{k}\Omega \]
- \[ \tan \max = 5.0 \text{k}\Omega \]
2. Improved Sample & Hold Stages

1) Employ composite CMOS transmission gate

\[ \text{Vin} \rightarrow V_{\text{out}} \]

r-channel and p-channel trans. are sized equally

- Opposite channel charges of p and n-channel trans. partially cancel each other

Problem: This works reasonably well for small input signals, where the 2 channel charges are closely matched.

For large signal swings, the 2 switching devices exhibit different effective voltages \((V_{\text{in}} - V_t)\), resulting in poor channel charge cancellation.

2) Add a Dummy Switch

\[ \text{Vin} \rightarrow M_1 \rightarrow M_2 \rightarrow V_{\text{out}} \]

\([C_{\text{in}}] \rightarrow C_{\text{d}}\]

Ma is chosen at half the size of \(M_1\) \((W_2 L_2)\) to accommodate half the channel charge of \(M_1\).

Problem: The channel charge of \(M_1\) does not equally divide into a left and right side portion, thus causing an incomplete channel charge elimination.
c) Differential S&H stage

This configuration eliminates common-mode errors such as offset. Gain errors, however, are not eliminated.

3. Active S&H circuits

A) S&H with unity-point buffer

- Buffer adds good driving capability.
- Gain error determined by passive circuit.
- Buffer adds additional offset error.
- Input is loaded by switch or resistor.
- Buffer requires high common-mode input range.
15. S/H with high input impedance

\[ V_{\text{out}} = \frac{A_1 \cdot A_2}{1 + A_1 \cdot A_2} \approx V_{\text{in}} \]

\[ V_{i_1} = -V_{\text{in}} \frac{A_1}{1 + A_1 \cdot A_2} = -V_{\text{in}} A_2 \quad \text{Small} \]

\[ V_{\text{out}_2} = V_{\text{out}_1} \]

\[ V_{i_2} = 0 \]

- \( \phi_1 \) active (loop closed) \( \rightarrow \) sample
- \( \phi_2 \) active (loop open) \( \rightarrow \) hold

Since the voltages on either side of the 2 switches are very small, charge injection errors are signal independent (offset only) and thus cause no distortion.

Problem 1: Speed is degraded due to the necessity to guarantee stability in the sampling mode (closed or open phase margin)
C) 5.4.1 H with Clock-feedthrough Cancellation

During the sampling mode (Q is active), the opamp acts in unity-gain configuration and the output tracks the input. In the hold mode, the input (x output) is stored across C1. Since both switches exhibit the same terminal voltages when they are turned off, the two clock-feedthrough errors are matched and suppressed by the common-mode rejection of the amplifier.

Note: The symmetry upon the switch turn-off time requires a comparatively low op-amp output impedance to match the source impedance of Vin.
D) Simple switched-capacitor S&H

- Sample mode ($Q_1$ is active)
  - Op-amp is in unity-gain mode
  - $V_{out} = 0$

- Hold mode ($Q_2$ is active)
  - $C_h$ acts as the op-amp feedback and preserves the stored charge $Q_1 = \text{Vin} \times C_h$
  - $V_{out} = \text{Vin}$

Note: This circuit is insensitive w.r.t. the op-amp offset voltage $V_{os}$

Explanation:

- $Q_1 = (\text{Vin} - V_{os}) \times C_h$ (for $Q_1$ active)
- $Q_2 = (V_{out} - V_{os}) \times C_h$ (for $Q_2$ active)

$Q_2 = Q_1 \Rightarrow V_{out} = V_{in}$ (charge preserved)
Problem: Since the op-amp output voltage is virtually zero during the sample and hold mode (i.e., $V_{out_1} = V_{in_1}$), a good slew rate is required to bring the output up to $V_{in}$ during the hold mode. Obviously, the output is only valid during $Q_2$.

\[ v_{out} = \frac{v_{in}}{1 + \frac{Q_1}{Q_2}} \]

E) Switched-capacitor S&H and lowpass filter.

This circuit realizes a unity-gain 1st-order lowpass filter with a cut-off frequency of

\[ f_{-3dB} = \frac{1}{2\pi f_{clock} C_2[1+Q_2]} \]

The output voltage shows a true S&H (stair) pattern, which reduces the op-amp slew rate requirement. However, the output is not offset compensated.