Objective:
Voltage Controlled Oscillators (VCOs) form central units in Phase-Locked-Loops (PLLs). PLLs can generate multiple outputs whose frequencies bear a prescribed relation (e.g. an integer multiple) to the frequency of a reference input. The output signals are typically generated by a VCO, which is controlled by the phase difference of the output to a fixed reference. PLL based frequency synthesizers are widely used in modern communication systems.

This lab presents an application of op-amps as building blocks in a nonlinear circuit. The particular VCO depicted in figure 1 generates a sawtooth shaped output ($V_2$) whose frequency is proportional to a control voltage $V_{ctl}$. As you may recognize, the first opamp in this circuit implements a continuous-time integrator while the second acts as a (voltage) comparator whose output is either high (≈ positive supply) or low (≈ negative supply). This binary output is used to control the analog switch, which periodically discharges the integrating capacitor.

Tasks:
1. Familiarize yourself with the data sheets of the LF353 dual JFET opamp chip and the MC14066 quad multiplexer/analog switch. Note that both chips will be operated with a supply of ±5 V. Pre-lab assignment.
2. Assume that the transmission gate depicted in figure 1 (¼ MC14066) is ideal, i.e., it shorts when $V_2$ exceeds $V_r$ and acts as an open circuit when $V_2$ is less than $V_r$. Furthermore, we expect $C_1$ to rapidly and completely discharge while $V_3$ is high. Compute the value of $V_r$ and try to sketch the expected time-domain waveforms of $V_2$ and $V_3$. Pre-lab assignment.
3. Considering the expected waveform of $V_2$, can you find a symbolic relationship between the RC time constant $\tau_1=R_1C_1$ of the integrator, the reference voltage $V_{ctl}$ and the resulting repetition rate or frequency of $V_2$? Pre-lab assignment.
4. If $R_1$ equals 100 kΩ and $V_{ctl}$=-2V, find a value for $C_1$ such that the frequency of $V_2$ approximates 5 kHz.
5. Simulate the VCO in PSpice using the opamp macro-model posted on the ele344 website. The transmission gate can be implemented either by an ideal switch (symbol S) or by a sufficiently wide n-channel MOS device yielding an on resistance of not more than 50 Ω.
6. Find a way to covert the sawtooth output to a square wave. If you have succeeded, increase the control voltage $V_{ctl}$ from -5 V to -1 V in steps of 0.5 V and record the resulting output frequency of $V_2$. How well does the $V_{ctl}$ versus $f_{out}$ relationship you derived in task 3 hold up?
7. Realize the sawtooth VCO on the Protoboard. After you have confirmed its proper operation, repeat the voltage versus frequency test you conducted in task 6. If you have 3 independent voltage sources at your disposal, you can use one source to directly alter the control voltage $V_{ctl}$, otherwise, vary $V_{ctl}$ by means of a potentiometer as shown in figure 1. Comment on the potential differences between simulation and measurement.

8. Can you find a purpose for the 50 nF load capacitance of the comparator? Observe how your outputs change if you remove this element and try to find and explanation for your observation.

9. Consider the oscillator in figure 2 and try to sketch the waveforms at outputs $V_2$ and $V_4$, respectively. Can you find the relationship between the frequency of $V_2$ or $V_3$ and the RC time constant $\tau_1=R_1C_1$?

10. Verify the expected performance of the oscillator depicted in figure 2 using PSpice. Comment on how closely your formula for the frequency of $V_2$ or $V_3$ holds up!

Figure 1: Voltage Controlled Oscillator generating a sawtooth output (node $V_2$) whose frequency is proportional to the control input $V_{ctl}$. The control voltage can be an independent source or, as shown, can be tuned with a potentiometer.

Figure 2: Alternative oscillator obtained by replacing the comparator in figure 1 by a Schmitt Trigger. The two MOS devices act as ideal switches, which connect the input to either $V_{DD}$ or $V_{SS}$. Note that $V_r$ is not constant in this circuit.