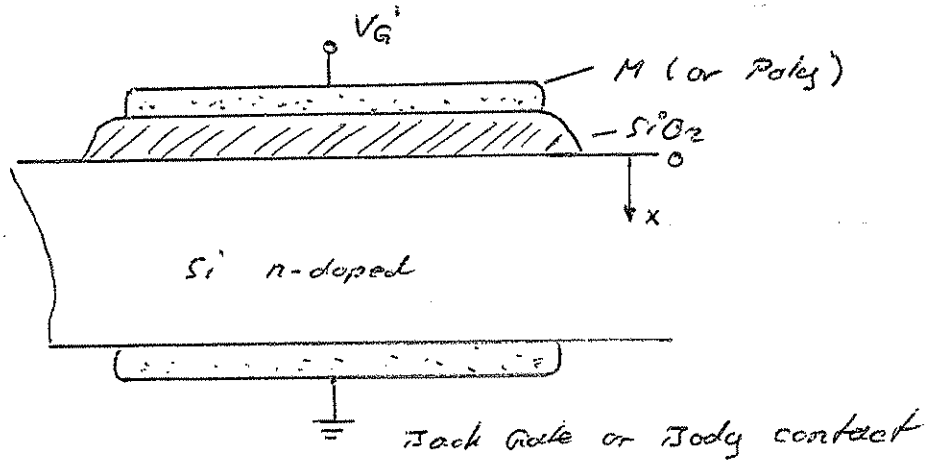
II. MOS Device Characteristics

1. The MOS Capacitor



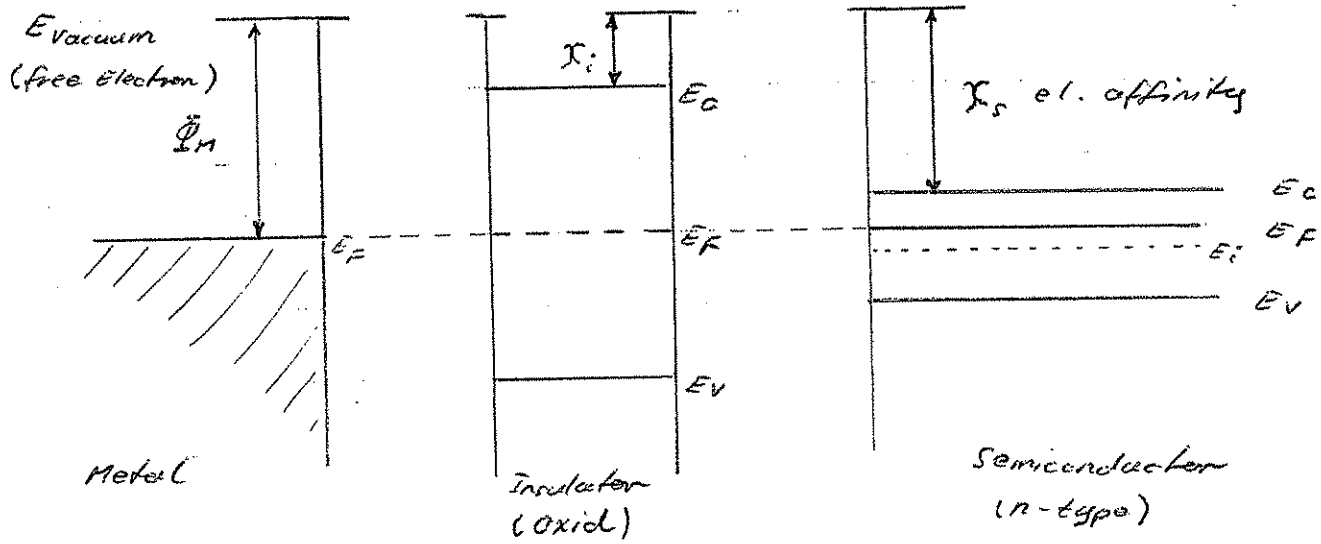
assumptions:

1. Gate is equipotential region
2. Oxide is perfect insulator
3. No charge centers in oxide
4. semiconductor is uniformly doped
5. Semic. is sufficiently thick so that a field-free region is formed before reaching the back contact
6. Back contact is ohmic
7. Capacitor is a one-dimensional structure in x
8. $\Phi_M = \chi_s + (E_C - E_F)$

Work fct. of Metal — el. affinity

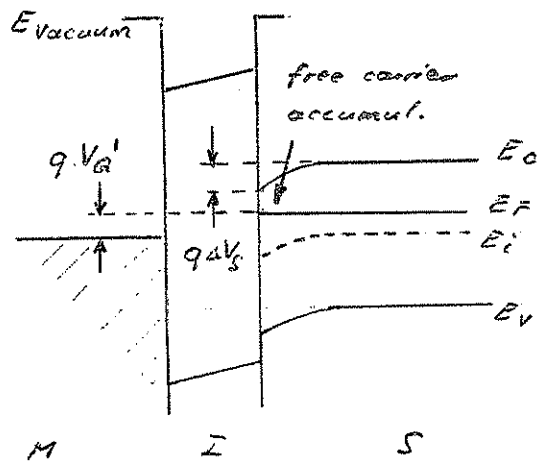
Energy-Band Diagrams

zero Bias ($V_G' = 0$)



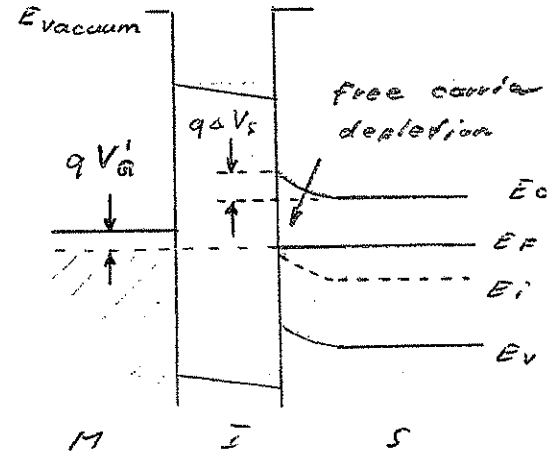
Nonzero Bias

a) $V_G' > 0$



ΔV_s: semiconductor surface potential

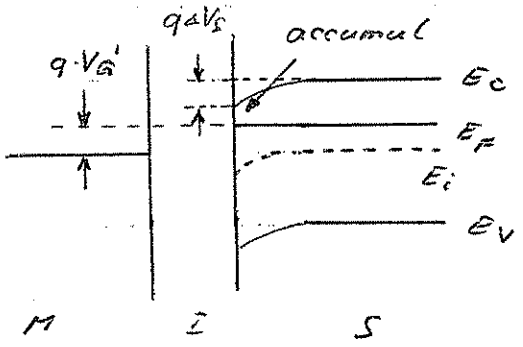
b) $V_G' < 0$ but $q\Delta V_s < (E_F - E_{i\infty})$

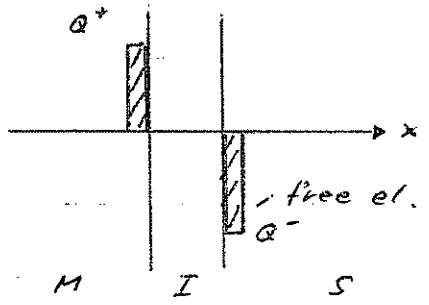


$E_{i\infty}$ denotes intrinsic Fermi level in field-free (bulk) Si

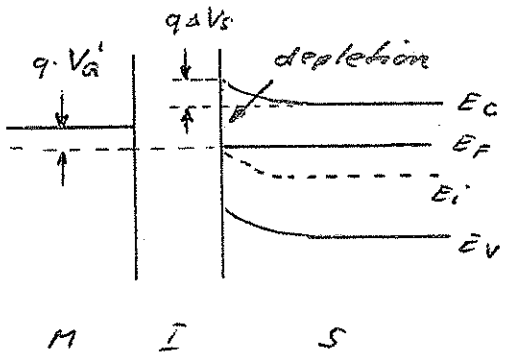
change distribution for different bias voltages

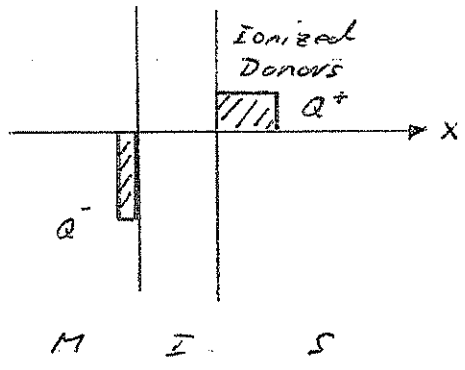
a) $V_G' > 0$



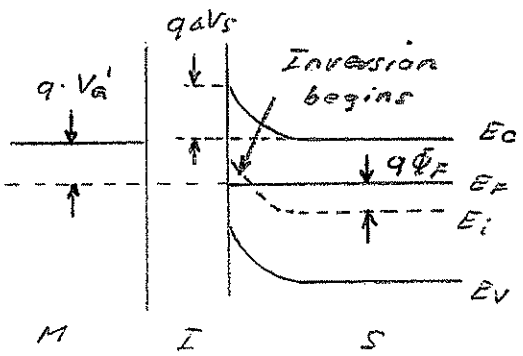


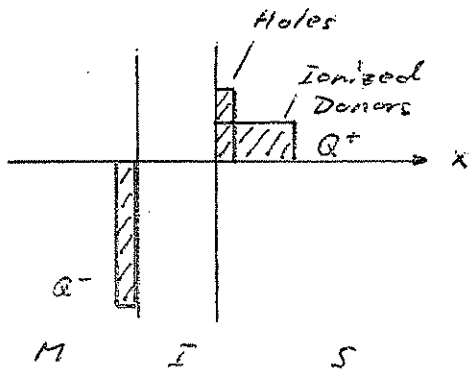
b) $V_G' < 0$ but $q\Delta V_S < (E_F - E_{i\infty})$





c) $V_G' < 0$ but $q\Delta V_S > (E_F - E_{i\infty})$





Inversion is achieved if

$$E_i(\text{surface}) - E_{i\infty} \geq 2\,(E_F - E_{i\infty})_{bulk} \qquad \text{Inversion (n-type S)}$$

or

$$-q\Delta V_s \geq 2\,(E_F - E_{i\infty})$$

The gate voltage V_G' that must be applied to achieve inversion is called Threshold voltage V_T'. Since $V_G' = \Delta V_{ox} + \Delta V_s$, we obtain:

$$V_T' = -2\frac{(E_F - E_{i\infty})}{q} + \Delta V_{ox} = +2\Phi_F + \Delta V_{ox} \qquad \text{(n-type S)}$$

Under inversion ($V_G' = V_T'$), the hole-concentration at the surface of the semiconductor is equal to the donor concentration N_D (Definition). Hence

$$p_s = N_D = n_i\, e^{\frac{(E_F - E_{i\infty})}{kT}} = n_i\, e^{-\frac{\Phi_F}{kT}}$$

$$W_T = \sqrt{\frac{2\varepsilon_s 2\Phi_F}{qN_D}}$$

and $\Delta V_{ox} = -\frac{Q_{dep}}{C_{ox}} = -\frac{q \cdot N_D \cdot W_T}{C_{ox}}$ $\qquad (C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}})$

Solving for Φ_F and V_T' yields:

$$\Phi_F = -\frac{kT}{q}\ln\left[\frac{N_D}{n_i}\right] \qquad \text{(n-type S)}$$

$$V_T' = +2\Phi_F - \frac{q \cdot N_D W_T}{C_{ox}} \qquad \text{p-channel device}$$

In analogy to this result, we obtain for a p-doped semicond.

$$\Phi_F = +\frac{kT}{q}\ln\left[\frac{N_A}{n_i}\right] \qquad \text{(p-type S)}$$

$$V_T' = +2\Phi_F + \frac{q N_A W_T}{C_{ox}} \qquad \text{n-channel device}$$

charge density distribution in MOS capacitor

The exact solution of the charge density distribution inside the semiconductor is obtained by solving Poisson's eq.

$$\left| \frac{dE}{dx} = \frac{\rho}{\varepsilon} \right|$$

where $\rho = q\,(p(x) - n(x) + N_D - N_A)$

$$\left| \begin{aligned} p(x) &= n_i\, e^{\frac{(E_i(x) - E_F)}{kT}} \\ n(x) &= n_i\, e^{\frac{(E_F - E_i(x))}{kT}} \\ N_D - N_A &= n_i \left[e^{-\frac{\Phi_F}{kT}} - e^{+\frac{\Phi_F}{kT}} \right] \end{aligned} \right|$$

Potential

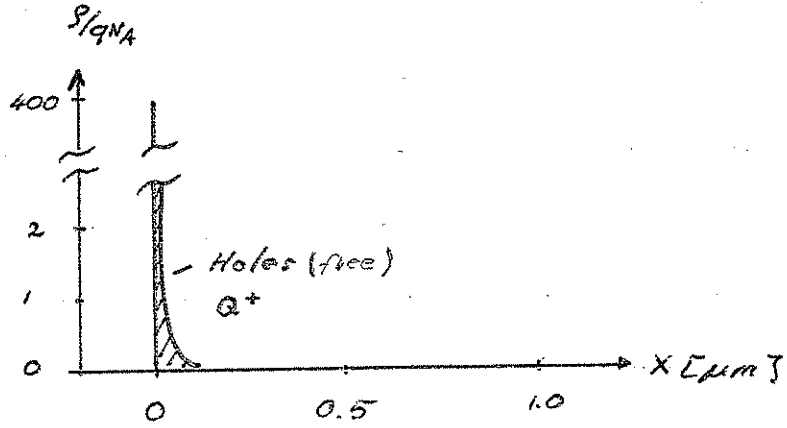
since $\rho = 0$ and $\Phi = 0$ in semiconductor bulk

Example: solution of Poisson's eq. for p-type Si with

$N_A = 10^{15}\,cm^{-3}$ $(\Phi_F = 0.3\,V)$

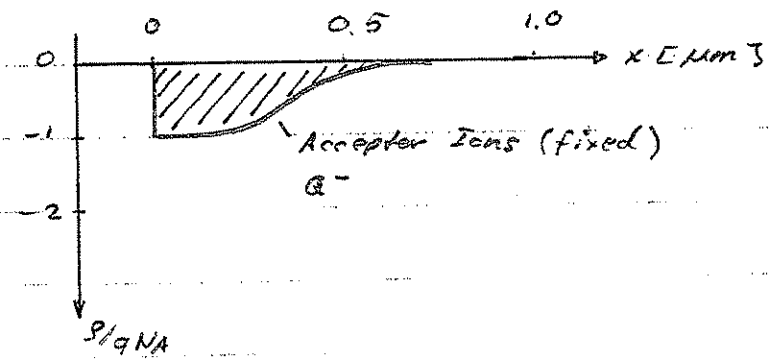
a) Accumulation

$\Delta V_S = -\frac{1}{2}\Phi_F$



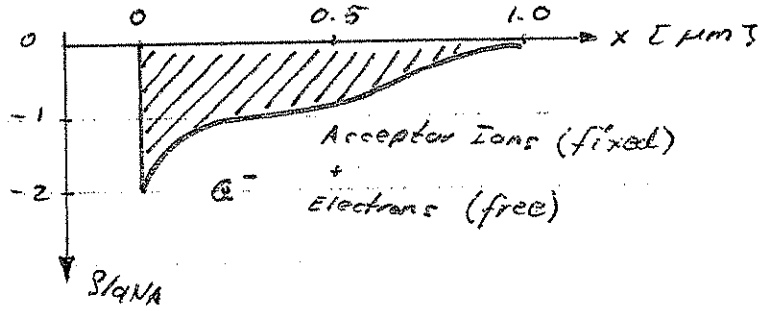
b) Depletion

$\Delta V_S = \Phi_F$



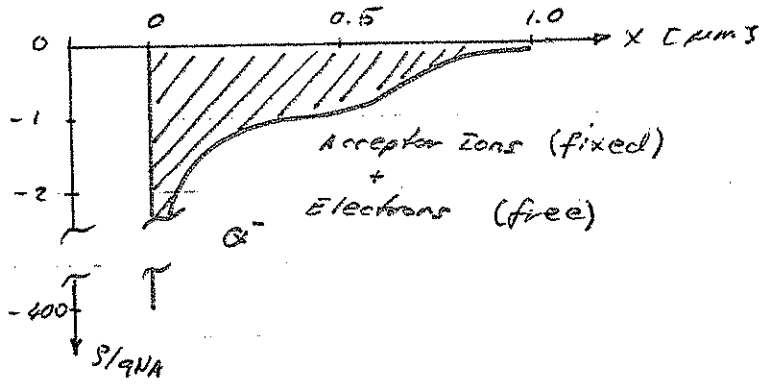
c) Onset of Inversion

$\Delta V_S = 2\,\Phi_F$



d) Deep Inversion

$\Delta V_S = 2.5\,\Phi_F$



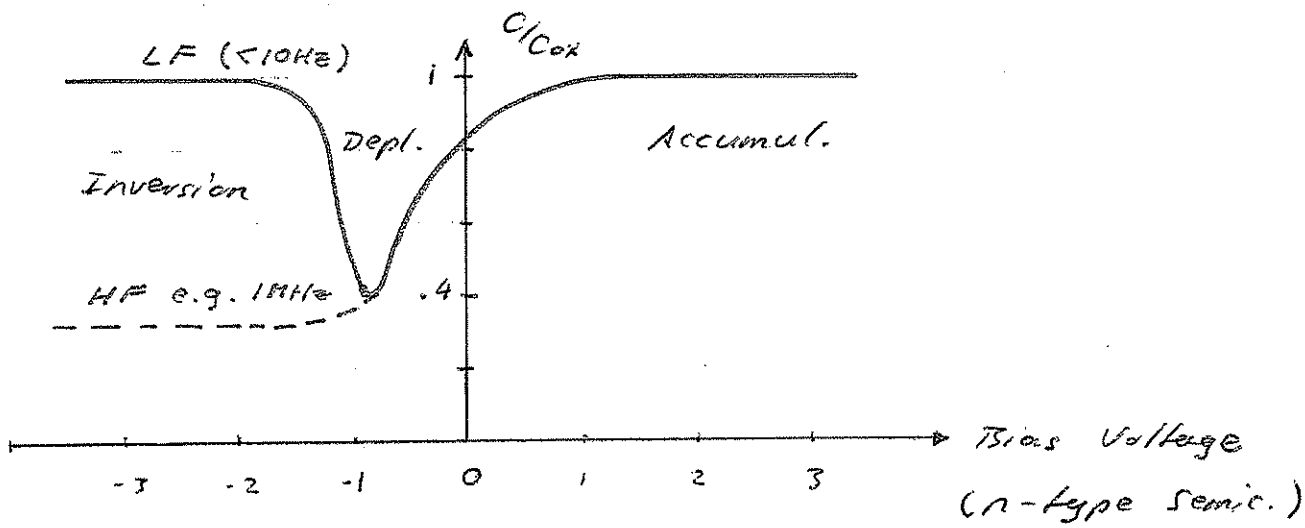
Note: The free charge carriers created through accumulation (holes in p-Si) or inversion (el in p-Si) reside in an extremely narrow portion of the semiconductor immediately adjacent to the oxide layer. By comparison, the depletion portion (acceptor ions in p-Si) extends much deeper into the semiconductor.

The depletion width at the onset of inversion is approximately given by:

$$W_T = \sqrt{\frac{2\varepsilon_s 2\phi_F}{q N_A}} \qquad (p\text{-type})$$

Note that the depletion width approx. remains constant if the bias voltage is increased above the threshold voltage.

Capacitance - Voltage Characteristics



Accumulation

$$C_{acc} \approx C_{ox} A_G = A_G \frac{\varepsilon_{ox}}{t_{ox}}$$

majority carrier

$\tau \approx 1ps$

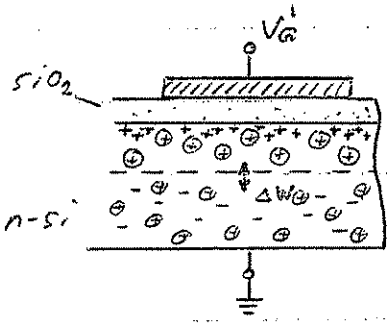
Notes $C_{ox} = \left[\frac{F}{m^2}\right]$

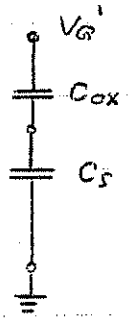
Depletion

$$C_{dep} \approx \frac{C_{ox} C_s}{C_{ox} + C_s}$$

ionized acceptors in depletion region

where $C_s = \varepsilon_s \frac{A_a}{W_T}$





$$C_{depl} = \frac{C_{ox}}{1 + \frac{\varepsilon_{ox}}{\varepsilon_S}\frac{W_T}{t_{ox}}}$$

depl. width is changed by changing el. concentration at the boundary between depl. region and the bulk semiconductor
→ involves majority carriers → short time const.

Inversion

In this case, charge variations in the semiconductor can be caused by small changes in the depletion width W (majority carriers → short time constant) or by changes in the inversion layer at the semiconductor - oxid interface (minority carriers must be generated → large time const.)
Thus, the effective capacitance under inversion depends on the frequency of the applied field

a) $\omega \to 0$

$$C_{inv} \approx C_{ox}$$

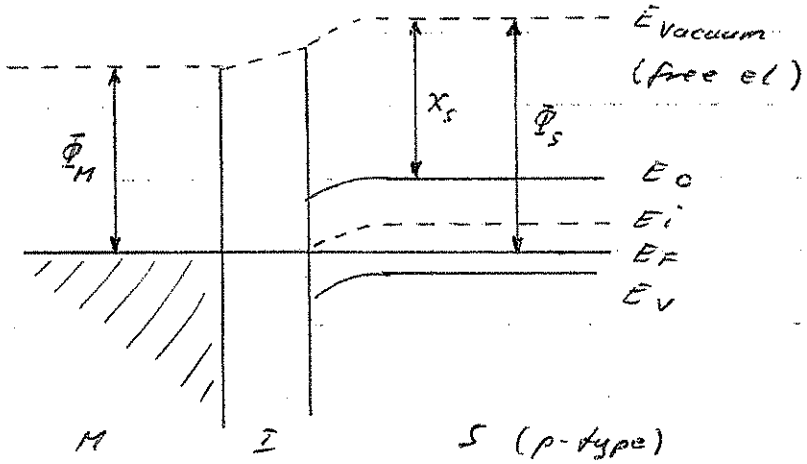
b) $\omega \to \infty$

$$C_{inv} \approx \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{depl}}} = \frac{C_{ox}}{1 + \frac{\varepsilon_{ox}}{\varepsilon_S}\frac{W_T}{t_{ox}}}$$

Deviations from the MOS Ideal

1.1. Metal - Semiconductor workfunction difference

Assumption 8), i.e. $\Phi_M = \chi_s + (E_c - E_F)$ is generally not true. In other words, the semiconductor does not exhibit a flat-band diagram under zero bias conditions. The exact band structure looks rather like



In order to achieve flat band conditions we must apply a certain gate voltage ΔV_{G1}, where

$$\Delta V_{G1} = V_{FB1} = \frac{1}{q}\left[\Phi_M - \Phi_S\right] = \frac{1}{q}\Phi_{MS} = \phi_{MS}$$

In most cases, V_{FB1} is negative and on the order of a few tenth of a volt (depending on doping conc. and semic. type)

1.2. Oxide charges

Mobile oxide charges (mostly Na^+)

Poisson's eq. $\frac{dE_{ox}}{dx} = \frac{\rho_{Mox}}{\varepsilon_{ox}}$ — mobile oxide charge per area

$$\Delta V_{G2_1} = V_{FB2_1} = -\frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} x \, \rho_{Mox} \, dx = -\gamma_M \frac{Q_M}{C_{ox}} \qquad (0 < \gamma_M < 1)$$

Effect reduced by "neutralization" of semiconductor - oxide interface e.g. by HCl, Cl_2 (Na^+ is neutralized by Cl^-)

Fixed oxide charges

From Poisson's eq. — positive ions

$$\Delta V_{G22} = V_{FB22} = -\frac{Q_{Fox}}{C_{ox}}$$

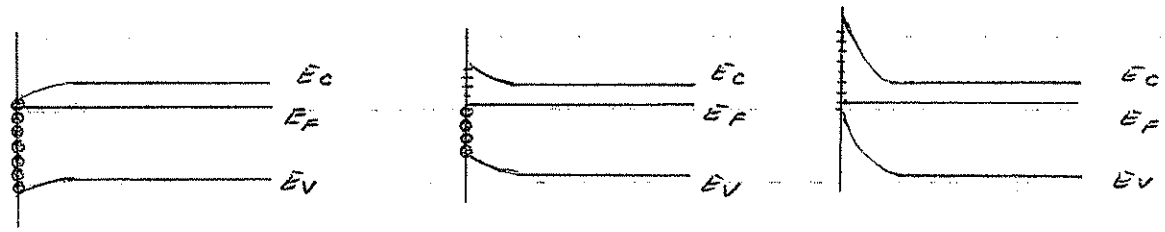
properties of Q_F:

1. Q_F is independent of t_{ox}
2. Q_F varies with Si surface orientation
3. Q_F is strong function of oxidation conditions
4. Annealing of oxidized Si in Ar or N_2 atmosphere reduces Q_F considerably

1.3. Interfacial Traps (or surface states)

Interfacial traps are allowed energy states in the band-gap in which electrons are "trapped" in the vicinity of the material's surface. They are created by "dangling bonds" at the semiconductor-oxide interface.

Example (n-type Si)



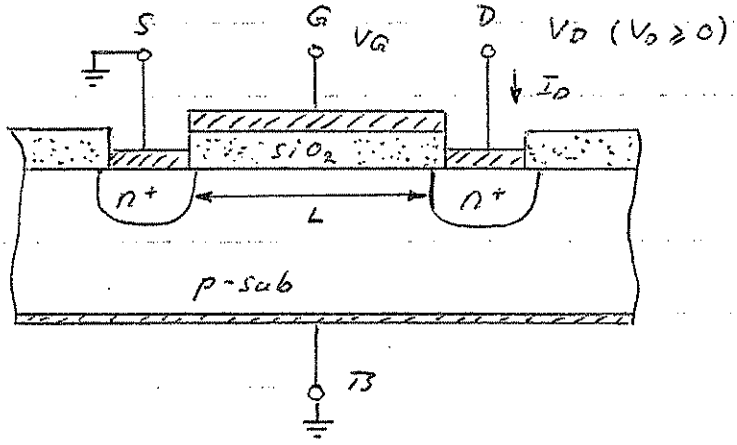
Since the charge Q_{SS} stored in the surface states, like Q_F, is located at the semiconductor-oxide interface, we can write, by direct analogy with the fixed oxide charge analysis,

$$\Delta V_{GS} = V_{FB_S} = -\frac{Q_{SS}}{C_{ox}} \qquad (\text{pos or neg})$$

Q_{SS} is very sensitive to even minor fabrication details and also depends on the orientation of the semiconductor surface.
The interfacial trap concentration can be minimized in one of two ways, namely, through post-metallization annealing or hydrogen (H_2) ambient annealing.

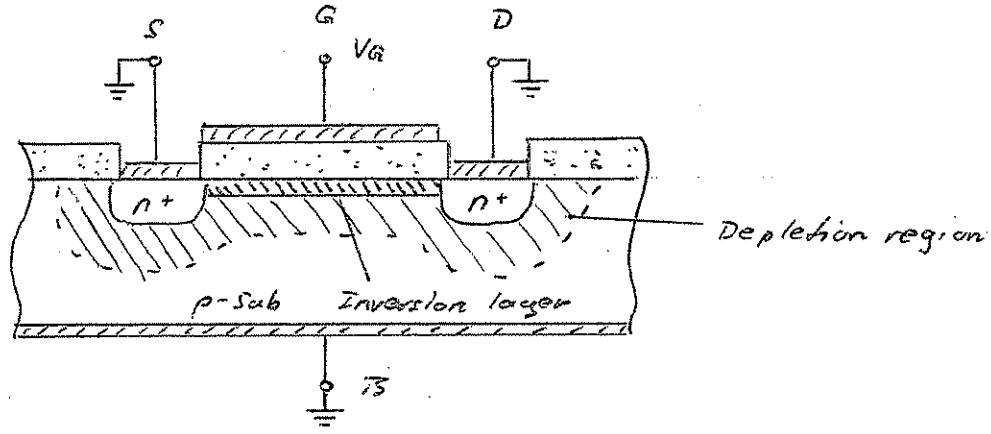
2. The MOS Fieldeffect Transistor

Basic Structure (n-channel)



Operation (enhancement-mode)

$V_G > V_T$ ($V_D = 0$)



Threshold voltage V_t: ($V_{SB} = 0$)

$$V_{t0} = V_{FB} + 2\phi_F + \frac{Q_{depl\,0}}{C_{ox}}$$ derived from MOS capacitor

where $V_{FB} = \phi_{MS} - \gamma_M \frac{Q_M}{C_{ox}} - \frac{Q_F}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}$ $\left(C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}\right)$

and $Q_{depl_0} = q N_A W_T = \sqrt{2 \varepsilon_S q N_A 2\phi_F}$ $\left(\phi_F = \frac{kT}{q} \ln\left[\frac{N_A}{n_i}\right]\right)$

$V_{SB} \neq 0$ (Body-Effect)

$$\begin{aligned} V_t &= V_{FB} + 2\phi_F + \frac{Q_{depl\,0}}{C_{ox}} + \frac{Q_{depl} - Q_{depl\,0}}{C_{ox}} \\ &= V_{t0} + \gamma\left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right] \\ &= V_{t0} + \gamma\sqrt{2\phi_F}\left[\sqrt{1 + \frac{V_{SB}}{2\phi_F}} - 1\right] \end{aligned}$$

where $\gamma = \frac{\sqrt{2 \varepsilon_S q N_A}}{C_{ox}}$ Body effect increases with $\sqrt{N_A} \cdot \frac{t_{ox}}{C_{ox}}$

and $V_{t0} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} = V_{FB} + \sqrt{2\phi_F}\left[\sqrt{2\phi_F} + \gamma\right]$

Example $N_A = 5 \cdot 10^{22}\ m^{-3}$

$V_{FB} = -0.6\,V$

$\phi_F = 0.4\,V$ $\Rightarrow$ $\gamma = 0.50\sqrt{V}$, $V_{t0} = 0.65\,V$

$\varepsilon_S = 10^{-10}\ \frac{As}{Vm}$

$C_{ox} = 2.5 \cdot 10^{-7}\ \frac{F}{m^2}$

$\therefore \gamma \cdot \sqrt{2\phi_F} = 0.45\,V$

$\therefore V_t(V_{SB}) = 0.65 + 0.45\left[\sqrt{1 + \frac{V_{SB}}{2\phi_F}} - 1\right]$

Quantitative Relationships

A) Square Law Theory (simple but not quite accurate)

current density in conducting channel:

$$J_y = q\mu_n n E_y = -q\mu_n n \frac{dV}{dy} \quad \text{(drift current)}$$

el mobility $\left[\frac{cm^2}{Vs}\right]$ $\quad \{\mu = \frac{v_d}{E}\}$

integrating the current density over cross sectional area of channel yields:

width W, depth x_0; channel width (z-direction)

$$I_D = +\int_0^W \int_0^{x_0} J_y \, dx \, dz = +W \int_0^{x_0} J_y \, dx$$

$$= \left(+W \frac{dV}{dy}\right)\left(-q \int_0^{x_0} \mu_n n \, dx\right) = -W \frac{dV}{dy} \mu_n \int q n \, dx$$

$$-\mu_n \cdot Q_N$$

Q_N: mobile charge in channel if $V_a > V_T$ (inversion layer)

since I_D is const. over full channel length, we can write:

$$\int_0^L I_D \, dy = I_D L = -W \mu_n \int_0^{V_D} Q_N \, dV$$

and finally

$$\boxed{I_D = -\mu_n \frac{W}{L} \int_0^{V_D} Q_N \, dV}$$

Calculation of channel charge Q_N:

assumption: charge added to the gate of an MOS-Cap is balanced by increases in the inversion layer charge ($V_{GS} \geq V_t$) — we assume $V_G = V_{ox} + 2\phi_F + V_{FB}$

Thus $-Q_N = Q_G\big|_{V_{GS} \geq V_t} = Q_G\big|_{V_{GS} = V_t}$ (onset of inversion)

$$= C_{ox}(\underbrace{V_{GS} - 2\phi_F - V_{FB}}_{\text{voltage between plates of Cap} = V_{ox0}}) - C_{ox}(V_t - 2\phi_F - V_{FB})$$

$$\Rightarrow \underline{Q_N = -C_{ox}(V_{GS} - V_t)}$$

$= V_{ox0}$

Finally, by replacing $(V_G - 2\phi_F - V_{FB})$ with $(V_{GS} - 2\phi_F - V_{FB} - V_S)$ where $0 \leq V \leq V_D$, we obtain:

$$\underline{\underline{Q_N(y) = -C_{ox}[V_{GS} - V_t - V(y)]}} \qquad (V_G \geq V_t)$$

and so

$$I_D = \mu_n \frac{W}{L} C_{ox} \int_0^{V_D} (V_{GS} - V_t - V_S)\, dV \qquad (0 \leq V_D \leq V_{Dsat})$$

$$= \mu_n \frac{W}{L} C_{ox} \left[(V_{GS} - V_t) \cdot V_D - \tfrac{1}{2} V_D^2\right] \qquad (V_G \geq V_t)$$

pre-pinch-off characteristics

post-pinch-off characteristics:

$$I_D\Big|_{V_D > V_{Dsat}} = I_D\Big|_{V_D = V_{Dsat}} = I_{Dsat} \quad \text{(assumption: current remains constant)}$$

or

$$\boxed{I_{Dsat} = \mu_n \frac{W}{L} C_{ox} \left[(V_G - V_t) V_{Dsat} - \frac{1}{2} V_{Dsat}^2 \right]}$$

Since $Q_N(L) = 0$ when $V_y(L) = V_{Dsat}$, we can write

$$Q_N(L) = -C_{ox} (V_{GS} - V_t - V_{Dsat}) = 0$$

$$\Rightarrow \underline{\underline{V_{Dsat} = [V_{GS} - V_t] = V_{eff}}}$$

$$\Rightarrow \boxed{I_D\Big|_{V_D \geq V_{Dsat}} = I_{Dsat} = \mu_n \frac{W}{L} C_{ox} \frac{1}{2} [V_{GS} - V_t]^2}$$

post-pinch-off characteristics

According to this eq., the saturation current varies as the square of the gate voltage above turn-on, the so called "square-law" dependence.

Channel Length Modulation

If $V_{DS} > V_{eff}$, the drain side of the conducting channel is pinched-off. The effective channel length is then given by

$$\boxed{L_{eff} = L - W_T(V_{DS})}$$

where $$W_T(V_{DS}) = \sqrt{\frac{2\varepsilon_s\varepsilon_0(\phi_0 + V_{DS} - V_{eff})}{q N_{sub}}}$$

$$\frac{dI_D}{dV_{DS}} = \frac{dI_D}{dL_{eff}}\frac{dL_{eff}}{dV_{DS}} = -\frac{1}{2}\frac{W}{L_{eff}^2}\mu C_{ox} V_{eff}^2 \frac{dL_{eff}}{dV_{DS}}$$

$$\frac{dL_{eff}}{dV_{DS}} = -\frac{dW_T}{dV_{DS}} = -\sqrt{\frac{\varepsilon_s\varepsilon_0}{2qN_{sub}(\phi_0 + V_{DS} - V_{eff})}}$$

$$\therefore \frac{dI_D}{dV_{DS}} = \underbrace{\frac{1}{2}\frac{W}{L}\mu C_{ox} V_{eff}^2}_{I_{D0}} \frac{1}{L_{eff}}\sqrt{\frac{\varepsilon_s\varepsilon_0}{2qN_{sub}(\phi_0 + V_{DS} - V_{eff})}}$$

$$\therefore \boxed{I_D(V_{DS}) = I_{D0}(1 + \lambda[V_{DS} - V_{eff}])}$$

where $$I_{D0} = \frac{1}{2}\frac{W}{L}\mu C_{ox} V_{eff}^2$$

$$\lambda = \frac{1}{L_{eff}}\sqrt{\frac{\varepsilon_s\varepsilon_0}{2qN_{sub}(\phi_0 + V_{DS} - V_{eff})}}$$

$$\boxed{I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{eff}^2(1 + \lambda[V_{DS} - V_{eff}])}$$

Subthreshold Conduction ($V_{GS} < V_t$)

(Berkeley Short channel Insulated-Gate FET Model)

In weak inversion, the current is due mainly to diffusion between the drain and the source, similar to the current of a BJT.

$$I_{D\,weak} = \frac{I_{exp} \cdot I_{limit}}{I_{exp} + I_{limit}}$$

where

$$I_{exp} \cong G \mu C_{ox} \frac{W}{L} (V_T)^2 e^{\frac{V_{GS} - V_t}{V_T}} \left[1 - e^{-\frac{V_{DS}}{V_T}}\right]$$

and

$$I_{limit} \cong \frac{q}{2} \mu C_{ox} \frac{W}{L} (V_T)^2 \qquad \left(V_T = \frac{kT}{q}\right)$$

If $V_{DS} > 2V_T$ then

$$I_{exp} \cong I_{no} \frac{W}{L} e^{\frac{V_{GS} - V_t}{V_T}} \qquad (V_{GS} < V_t)$$

where

$$I_{no} \cong G \mu C_{ox} (V_T)^2$$

e.g. $T = 300°K$

$C_{ox} = 2.5 \times 10^{-7} \frac{F}{m^2}$ $\quad \therefore I_{no} \cong 400\,nA$

$\mu_n = 4 \times 10^{-2} \frac{m^2}{Vs}$

$V_{GS} - V_t = -2V_T = -52\,mV$

$\frac{W}{L} = 2$ $\quad \therefore I_{exp} \cong 108\,nA$

Device Models

MOS Transistor in ohmic region

$V_{GS} < V_t$: $I_D = 0$ $\quad r_d \to \infty$

$V_{GS} \geq V_t$: $I_D = \frac{W}{L} \mu C_{ox} \left[V_{GS} - V_t - \frac{1}{2} V_{DS} \right] V_{DS}$

channel conductance $g_d = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}}$

$$\boxed{g_d = \frac{W}{L} \mu C_{ox} \left[V_{GS} - V_t - V_{DS} \right]}$$

if $V_{DS} << V_{GS} - V_t$ $\quad g_d = \frac{W}{L} \mu C_{ox} \left[V_{GS} - V_t \right]$

voltage controlled resistor / conductor

example: $V_{GS} - V_t = 1V \gg V_{DS}$

$\mu_n = 4 \cdot 10^{-2} \frac{m^2}{Vs}$

$C_{ox} = 2.5 \cdot 10^{-3} \frac{F}{m^2}$ $\quad \Rightarrow \quad g_d = 40 \cdot 10^{-5} S$

$\frac{W}{L} = 4$

$r_d = 2.5 \, K\Omega$

Note: If the MOS transistor is used as a switch, r_d represents the switch-on resistance r_{on}.

MOS Transistor in Saturation

$V_{GS} \geq V_t$ inversion condition

$V_{DS} \geq (V_{GS} - V_t)$ saturation condition

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_{ox}[V_{GS} - V_t]^2 (1 + \lambda[V_{DS} - V_{eff}])$$

($V_{eff} = V_{GS} - V_t$)

1. channel conductance $g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}}$

$$\boxed{g_d = \frac{1}{2}\frac{W}{L}\mu C_{ox}[V_{GS} - V_t]^2 \lambda = I_D \cdot \lambda}$$

2. transconductance $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS} = V_{eff}}$

$$\boxed{g_m = \frac{W}{L}\mu C_{ox}[V_{GS} - V_t] = \sqrt{2\frac{W}{L}\mu C_{ox} I_D}}$$

e.g. $\mu C_{ox} = 10^{-4}\ \frac{A}{V^2}$

$V_{GS} - V_t = V_{eff} = 100mV$

$\frac{W}{L} = 10$

$\boxed{\begin{array}{l} I_D = 5\mu A \\ g_m = 10^{-4} S \end{array}}$

3. back gate transconductance $g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = -\frac{\partial I_D}{\partial V_{SB}}$

$$\boxed{g_{mb} = -\frac{\partial I_D}{\partial V_t}\frac{\partial V_t}{\partial V_{SB}} = g_m \frac{\partial V_t}{\partial V_{SB}}}$$

Recall: $V_t = V_{to} + \gamma[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}]$

$$\frac{\partial V_t}{\partial V_{SB}} = \frac{1}{2}\gamma\frac{1}{\sqrt{2\phi_F + V_{SB}}} \quad \text{where} \quad \gamma = \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_A}$$

$$\Rightarrow \boxed{g_{mb} = g_m \frac{1}{C_{ox}}\sqrt{\frac{\varepsilon_s q N_A}{2(2\phi_F + V_{SB})}}}$$

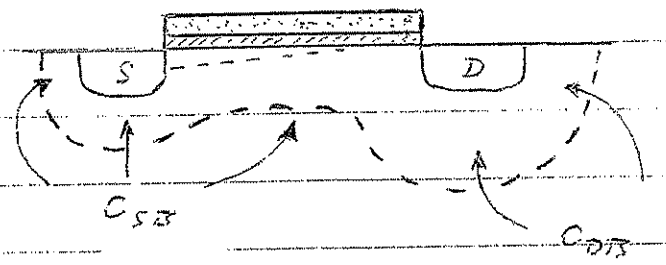
4 Capacitances

4.1 Junction Capacitances

a) $C_{SB} = \dfrac{C_{SB0}}{\sqrt{1 + V_{SB}/\phi_0}}$ where $\phi_0 = \dfrac{kT}{q}\ln\left[\dfrac{N_A \cdot N_D}{n_i^2}\right]$ built-in potential across S-B or D-B junction

$C_{SB0} = \sqrt{\dfrac{q\varepsilon_s N_{sub}}{2\phi_0}}\ \left[\dfrac{F}{m^2}\right]$

b) $C_{DB} = \dfrac{C_{DB0}}{\sqrt{1 + V_{DB}/\phi_0}}$

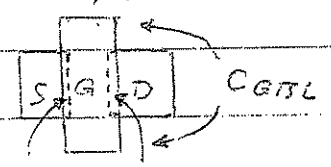


4.2 Overlap Capacitances

a) Gate - Bulk overlap capacitance C_{GBL}

(Parasitic ox. cap. between Gate and Substrate outside Device area)

Const. cap. on the order of 10 - 100 fF Poly



b) Gate - Drain and Gate - Source overlap C_{GDL} C_{GSL}

Capacitances C_{GDL} and C_{GSL}

Const. cap. on the order of 1 - 10 fF (empirical)

$C_{GDL} = C_{GSL} = \frac{2}{4} W X_j C_{ox}$

4.3 Channel Capacitances (for saturation)

a) $C_{GSC} = \dfrac{\partial Q}{\partial V_{GS}}$ $\quad Q_T$: total charge stored in channel

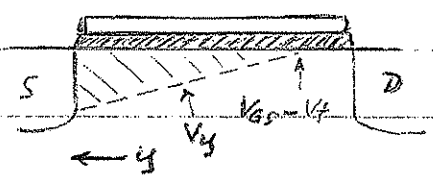
$$Q_T = W \cdot C_{ox} \int_0^L [V_{GS} - V_t - V(y)]\, dy$$

since $dR = \dfrac{d(V(y))}{I_D} = \dfrac{dy}{W \mu_n C_{ox} [V_{GS} - V_t - V(y)]}$ $\quad dR = \dfrac{dy}{W} \cdot R_D$

or $dq = W \mu_n C_{ox} [V_{GS} - V_t - V(y)] \dfrac{dV(y)}{I_D}$

$$\Rightarrow Q_T = W^2 \mu_n C_{ox}^2 \int_0^{V_{GS}-V_t} \underbrace{[V_{GS} - V_t - V(y)]^2}_{\frac{1}{3}[V_{GS}-V_t]^3} \frac{dV(y)}{I_D}$$

$$= \frac{2}{3} W \cdot L \cdot C_{ox} [V_{GS} - V_t]$$



$$\underline{\underline{C_{GSC} = \frac{2}{3} W \cdot L \cdot C_{ox}}}$$

b) $C_{GDC} = \dfrac{\partial Q_T}{\partial V_{GD}} \approx 0$ (except for very small L)

Summary of small signal 1st order model in saturation

Resistive Parameters:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \frac{W}{L}\mu C_{ox}[V_{GS} - V_T] = \sqrt{2\frac{W}{L}\mu C_{ox} I_D}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} \approx g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \gamma\sqrt{\frac{\frac{W}{L}\mu C_{ox} I_D}{2(2\Phi_F + V_{SB})}}$$

$$\gamma = \frac{1}{C_{ox}}\sqrt{2\varepsilon_S q N_A}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \approx \frac{1}{2}\frac{W}{L}\mu C_{ox}[V_{GS} - V_T]^2\lambda = I_D \cdot \lambda$$

Capacitive Parameters:

$$C_{SB} = \frac{C_{SB0}}{\sqrt{1 + V_{SB}/\Phi_0}}$$

$$C_{DB} = \frac{C_{DB0}}{\sqrt{1 + V_{SB}/\Phi_0}}$$

C_{GB}: Parasitic oxide cap.
$\approx$ 1 - 10 fF

$$C_{GS} = C_{GSC} + C_{GSL}$$
$$\approx \frac{2}{3} W L C_{ox}\left(1 + \frac{3 \cdot x_d}{2 \cdot L}\right)$$

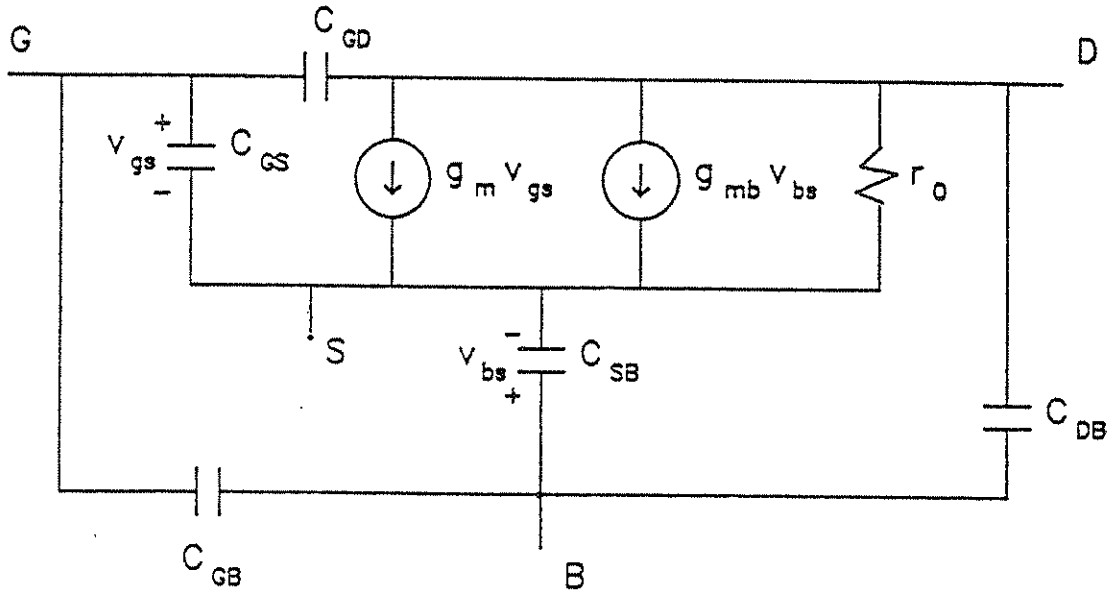
$$C_{GD} \approx C_{GDC} = C_{GSL}$$
$$= \frac{2}{4} W x_j C_{ox}$$

$$\Phi_0 = \frac{kT}{q} \ln\left[\frac{N_A \cdot N_D}{n_i^2}\right] \approx 0.9V$$

$$C_{SB0} = C_{DB0} = \sqrt{\frac{q \varepsilon_S N_{sub}}{2\Phi_0}} \approx 7 \times 10^{-4} \frac{F}{m^2}$$

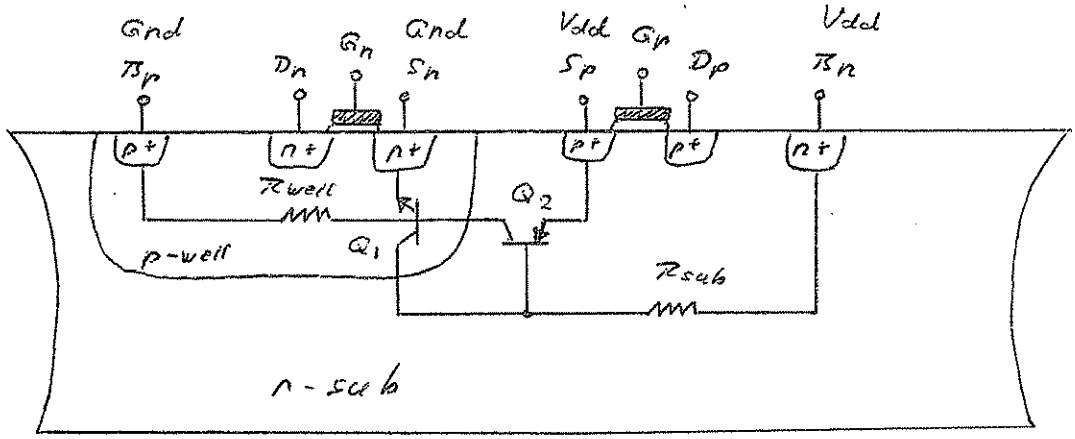
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \approx 2.5 \cdot 10^{-3} \frac{F}{m^2}$$

C. MODEL – SMALL SIGNAL IN SATURATION



Latchup in Bulk CMOS

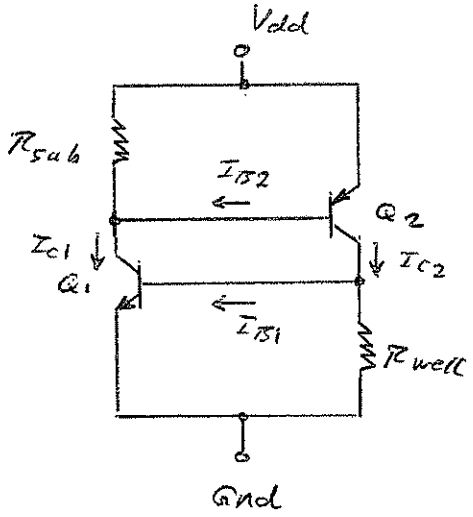
Example p-well process



Q_1 : vertical npn transistor (n-sub / p-well / S_n)
C B E

Q_2 : lateral pnp transistor (p-well / n-sub / S_p)
C B E

Parasitic Circuit:



equation system
(Q_1 and Q_2 op. in forw. active mode)

$$\left| \begin{array}{l} V_{BE1} = (I_{C2} - I_{B1})\, R_{well} \\ V_{BE2} = (I_{C1} - I_{B2})\, R_{sub} \end{array} \right|$$

$$\left| \begin{array}{l} I_{C1} = \beta_1 I_{B1} \\ I_{C2} = \beta_2 I_{B2} \end{array} \right|$$

Total current from Vdd to Gnd $I_{tot} = I_{C1} + I_{C2}$

eliminating I_{c1} and I_{c2} yields:

$$V_{BE1} = (\beta_2 I_{B2} - I_{B1})\, r_{well}$$

$$V_{BE2} = (\beta_1 I_{B1} - I_{B2})\, r_{sub}$$

Finally, we can solve for I_{B1} and I_{B2}

$$I_{B1} = \frac{1}{(\beta_1\beta_2 - 1)}\left[V_{BE1}\frac{1}{r_{well}} + V_{BE2}\frac{\beta_2}{r_{sub}}\right]$$

$$I_{B2} = \frac{1}{(\beta_1\beta_2 - 1)}\left[V_{BE1}\frac{\beta_1}{r_{well}} + V_{BE2}\frac{1}{r_{sub}}\right]$$

Conclusion: In order to avoid latchup, Q_1 and Q_2 must not be operated in the forward active mode! This condition is guaranteed if $\beta_1\beta_2 < 1$. (I_{B1} and I_{B2} become negative)

The current gains β_1 and β_2 of the parasitic BJT's are lowered if the width of their corresponding base regions are increased (min. distance between n-ch. and p-ch. devices; min. well depth).
Latchup can also be avoided by placing the substrate contacts next to the source diffusions, thus effectively shorting the B-E junctions of the parasitic BJT's.