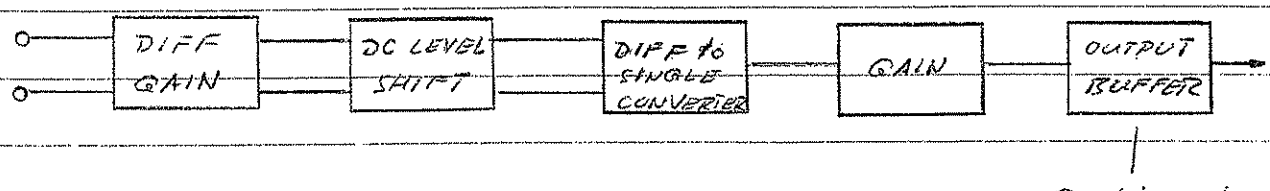
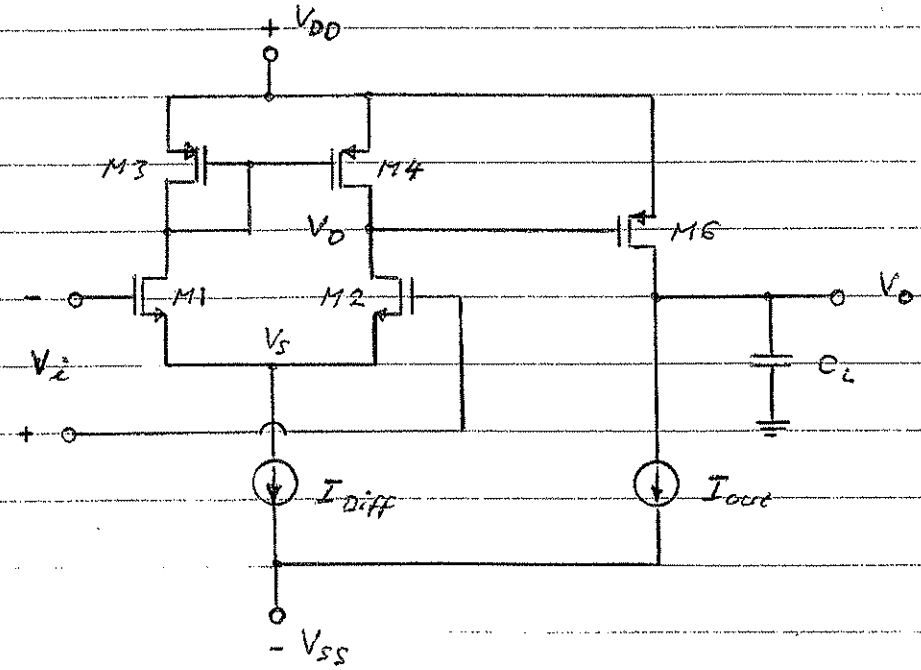
IV Operational Amplifiers and Comparators

1. Overview

Opamp internal functions

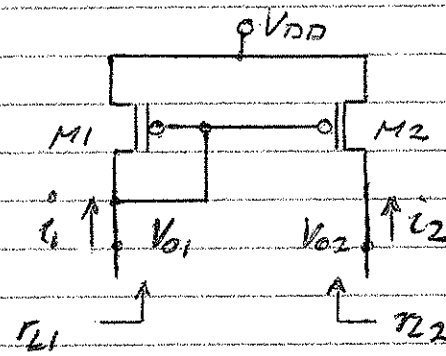


Basic 2-Stage CMOS Opamp



Differential to Single-ended Conversion

Basic Configuration (p-channel Load)

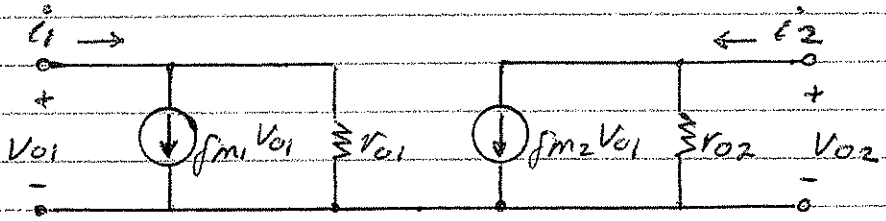


DC symmetry $\therefore g_{m1} = g_{m2}$

AC Differential mode

$\therefore \boxed{i_1 = -i_2}$

Linear equivalent circuit ($V_{DD} \triangleq$ Gnd)



DC symmetry

$r_{o1} = r_{o2}$

$g_{m1} = g_{m2}$

Equations

$$V_{o1} = (i_1 - g_{m1} V_{o1}) r_{o1} \quad (1)$$

$$V_{o2} = (i_2 - g_{m2} V_{o1}) r_{o2} \quad (2)$$

$$i_1 = -i_2 \quad (3)$$

From (1) $\quad \boxed{r_{L1} = \frac{V_{o1}}{i_1} = \frac{r_{o1}}{1 + g_{m1} r_{o1}} \cong \frac{1}{g_{m1}}}$

(1)+(2) $\quad \boxed{V_{o2} = \left(i_2 - i_1 \frac{g_{m2} r_{o1}}{1 + g_{m1} r_{o1}}\right) r_{o2}} \quad (4)$

(3)+(4) $\quad \boxed{\frac{V_{o2}}{i_2} = r_{L2} = \left(1 + \frac{g_{m2} r_{o1}}{1 + g_{m1} r_{o1}}\right) r_{o2} \cong 2 r_{o2}} \quad (5)$

Diff. Gain: $\quad \boxed{\begin{aligned} V_{o1_{dm}} &= -\tfrac{1}{2} V_{dm} g_{m_{in}} r_{L1} \cong -\tfrac{1}{2} V_{dm} \frac{g_{m_{in}}}{g_{m1}} \\ V_{o2_{dm}} &= \tfrac{1}{2} V_{dm} g_{m_{in}} r_{L2} \cong V_{dm} g_{m_{in}} r_{o2} \end{aligned}}$

Note: Under common mode (cm) input conditions, eq. (3) has to be replaced by

$$\boxed{i_{1cm} = i_{2cm} = \frac{1}{2}\frac{V_{cm}}{r_{55}}} \qquad (3')$$

where r_{55} denotes the output resistance of the tail current source I_{55}.

Equation (5) thus changes to

$$\boxed{\frac{V_{o2}}{i_{2cm}} = r_{2cm} = \left(1 - \frac{g_{m2}r_{01}}{1+g_{m1}r_{01}}\right) r_{02} \cong \frac{1}{g_{m1}}} \qquad (5')$$

Therefore

$$\boxed{\begin{aligned} V_{o1cm} &= \frac{1}{2} V_{cm} \frac{r_{21}}{r_{55}} = \frac{1}{2} V_{cm} \frac{1}{g_{m1} r_{55}} \\ V_{o2cm} &= \frac{1}{2} V_{cm} \frac{r_{22}}{r_{55}} \cong \frac{1}{2} V_{cm} \frac{1}{g_{m1} r_{55}} \end{aligned}}$$

Summary

Diff. Gain	$A_{dm} = g_{m_{in}} r_{02}$
CM Gain	$A_{cm} = \frac{1}{2}\frac{1}{g_{m1} r_{55}}$
CMRR	$\frac{A_{dm}}{A_{cm}} = 2 g_{m_{in}} r_{02} g_{m1} r_{55}$

2 Design for DC

A) DC Biasing ($V_i = 0$)

$$\frac{1}{2} I_{Diff} = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L}\right)_1 [V_{GS1} - V_{t1}]^2$$

$$V_{GS1} = -V_S \qquad (V_{i1} = V_{i2} = 0)$$

$$\Rightarrow \underline{\underline{V_S = -\left[V_{t1} + \sqrt{\frac{I_{Diff}}{\mu C_{ox} (W/L)_1}}\right]}}$$

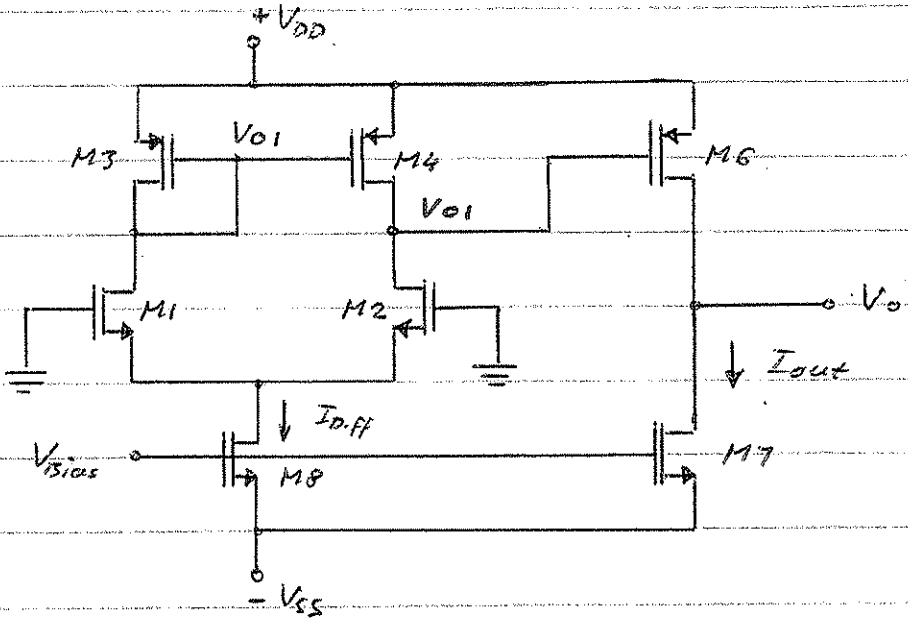
$$\frac{1}{2} I_{Diff} = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L}\right)_3 [-V_{GS3} + V_{t3}]^2$$

$$V_{GS3} = -(V_{DD} - V_D)$$

$$\Rightarrow \underline{\underline{V_D = V_{DD} - \left[-V_{t3} + \sqrt{\frac{I_{Diff}}{\mu C_{ox} \left(\frac{W}{L}\right)_3}}\right]}}$$

Notes: To achieve a large input common mode range keep V_S close to zero and V_D close to V_{DD}. ⟶ choose a small value for I_{Diff}. As we shall see, this also yields a max Gain. The price for these improvements is a reduction in the amplifier speed.

13) Systematic offset Voltage



To obtain zero systematic offset, $V_o\big|_{V_{G1}=V_{G2}} = 0$. This implies that $I_3 = I_4 = \frac{1}{2} I_{Diff}$

Since M3, M4 and M6 are all p-type transistors with the same V_{GS}, we can write:

$$\left| \frac{I_{Diff}}{I_{out}} = \frac{2(W/L)_3}{(W/L)_6} = \frac{2(W/L)_4}{(W/L)_6} \right| \qquad (1)$$

Similar arguments applied to M7 and M8 yields

$$\left| \frac{I_{Diff}}{I_{out}} = \frac{(W/L)_8}{(W/L)_7} \right| \qquad (2)$$

Thus, to achieve zero systematic offset, we must satisfy the following equation:

$$\left\| \frac{2(W/L)_3}{(W/L)_6} = \frac{2(W/L)_4}{(W/L)_6} = \frac{(W/L)_8}{(W/L)_7} \right\|$$

c) Random Offset Voltage

If offsets in V_t and $\left(\frac{W}{L}\right)$ in the differential input stage only are considered, a straightforward analysis gives:

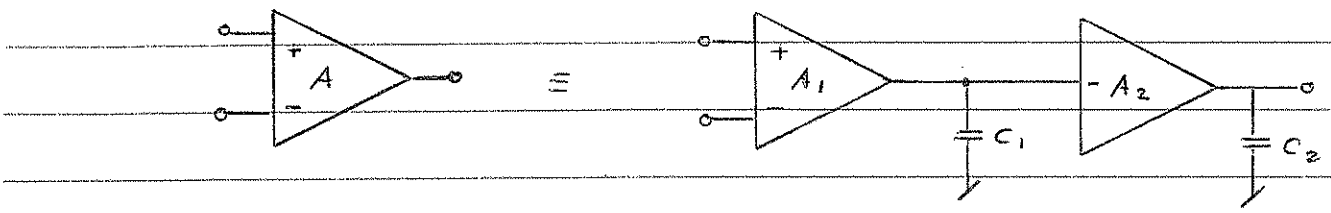
$$V_{OS} = \Delta V_{t_{1-2}} + \Delta V_{t_{3-4}} \frac{g_{m3-4}}{g_{m1-2}} + \frac{1}{2}\underbrace{[V_{GS} - V_t]_{1-2}}_{\sqrt{\frac{I_{D1/2}}{K_{1-2}}}}\left[\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}}\right]$$

- $\Delta V_{t_{1-2}}$: Mismatch of Input V_t
- $\Delta V_{t_{3-4}} \frac{g_{m3-4}}{g_{m1-2}}$: Mismatch of Loads reduced by g_{m3}/g_{m1}
- $\frac{1}{2}[V_{GS} - V_t]_{1-2}$: $\sqrt{\frac{I_{D1/2}}{K_{1-2}}}$
- $\left[\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}}\right]$: (W/L) Mismatch of Inputs + Loads

- Operate input stage at low bias to minimize offset
- Realize small ratio of g_{m3}/g_{m1}

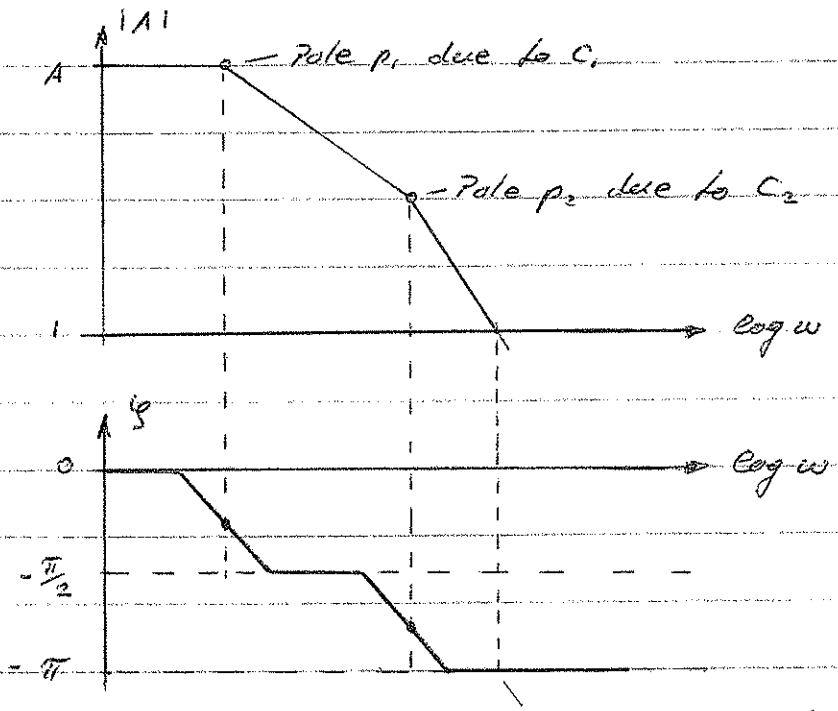
5. Design for AC

A) Compensation



$A = A_1 \cdot A_2$ $\quad$ C_1, C_2: Parasitic Capacitances

Gain Phase Plot



Opamp in Feedback Configuration:

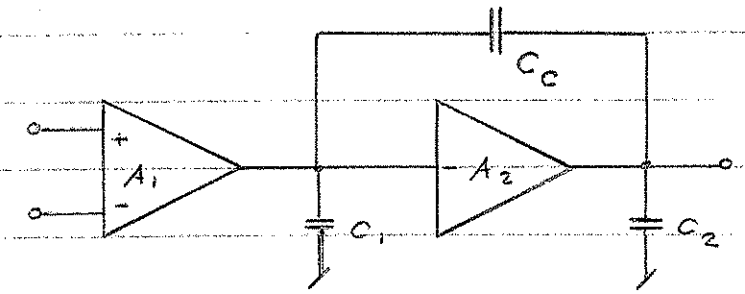
- 180° Phase shift due to neg. feedback
- 180° Phase shift due to parasitic poles

⇒ total phase shift: 360° i.e. neg. feedback becomes <u>positive</u>

⇒ instability

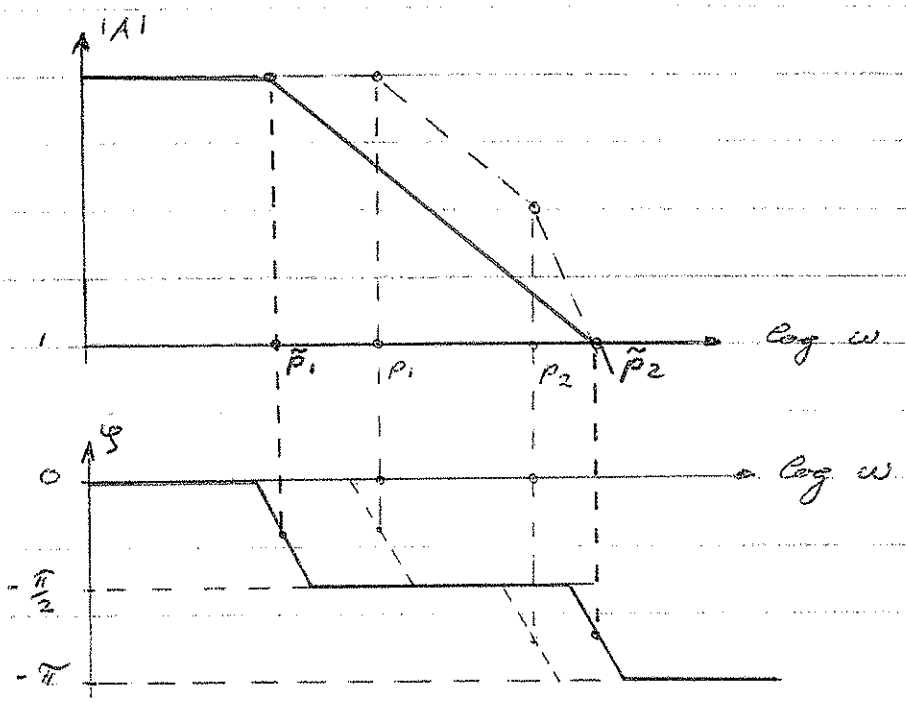
⇒ Additional phase compensation required

Pole Splitting Compensation



C_c pushes pole 1 lower in frequency due to Miller multiplication

pushes pole 2 higher in frequency

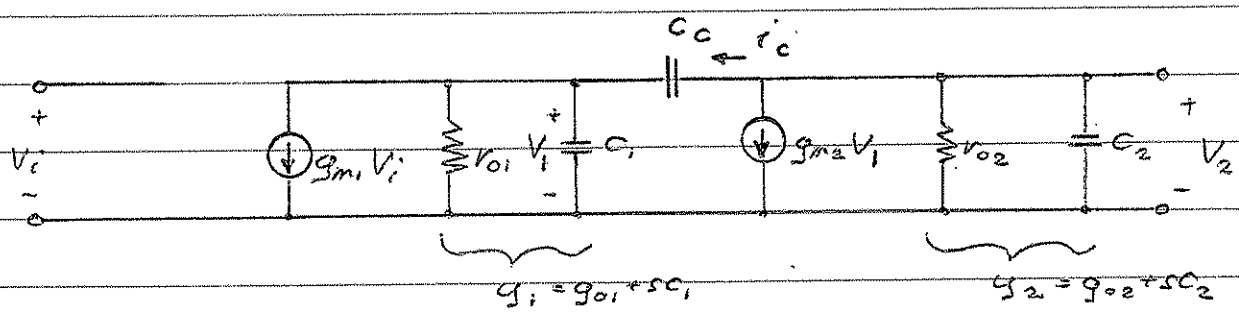


at $|A| = 1$ $\quad \varphi = -\frac{5}{4}\pi$

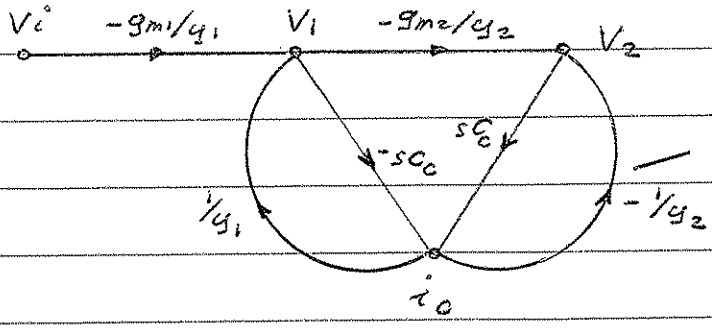
$\Rightarrow$ Phase margin: $+\frac{1}{4}\pi \hat{=} 45°$

Quantitative Description

Small Signal model of Opamp



SFG



this feedback is eliminated with a source follower in the C_c branch and sC_c has to be replaced by $\frac{sC_c}{1+\frac{sC_c}{g_{m2}}}$

$$\Rightarrow \frac{V_2}{V_i} = \frac{g_{m1}(g_{m2} - sC_c)\cdot\left(1+\frac{sC_c}{g_{m2}}\right)}{y_1 y_2 + sC_c(g_{m2} + y_1 + y_2)} \qquad \left(1+\frac{sC_c}{g_{m2}}\right) \text{ cancels}$$

$$\frac{V_2}{V_i} = \frac{g_{m1}g_{m2}}{g_{o1}g_{o2}} \frac{\left(1 - s\frac{C_c}{g_{m2}}\right)}{\left(1 + s\left[\frac{C_1}{g_{o1}} + \frac{C_2}{g_{o2}} + \frac{C_c}{g_{o1}} + \frac{C_c}{g_{o2}} + \frac{C_c g_{m2}}{g_{o1}g_{o2}}\right] + s^2\left(\frac{C_1C_2}{g_{o1}g_{o2}} + C_c\frac{C_1+C_2}{g_{o1}g_{o2}}\right)\right)}$$

Source Follower

		Note: without C_c ($C_c = 0$)
Zero:	$\tilde{z}_1 = \frac{g_{m2}}{C_c} \quad -\frac{g_{m2}}{C_c}$	$z_1 \to \infty$
Poles:	$\tilde{p}_1 \cong -\frac{g_{o1}g_{o2}}{g_{m2}C_c}$	$p_1 = -\frac{g_{o1}}{C_1} = \tilde{p}_1 \frac{C_c}{C_1}\frac{g_{m2}}{g_{o2}}$
	$\tilde{p}_2 \cong -\frac{g_{m2}C_c}{C_1C_2 + C_c(C_1+C_2)}$	$p_2 = -\frac{g_{o2}}{C_2} = \tilde{p}_2\left(1+\frac{C_1}{C_2}+\frac{C_1}{C_c}\right)\frac{g_{o2}}{g_{m2}}$
	$\tilde{p}_3 \cong -\frac{g_{m2}}{C_1} \quad \tilde{p}_3 \cong -\frac{1}{C_1R_2}$	$\tilde{p}_1 = p_1\frac{C_1}{C_c}\frac{g_{o2}}{g_{m2}}$
		$\tilde{p}_2 = p_2\frac{1}{(1+C_1/C_2+C_1/C_c)}\frac{g_{m2}}{g_{o2}}$

Right-Half-plane zero: Adds additional neg. phase to transfer function
⇒ decreases phase margin

Solution: zero must be shifted over to left half-plane
⇒ phase margin is increased

A) with a Source-Follower in the feedback path

zero: $\boxed{\tilde{z}_1' \to \infty}$

eliminates RHP zero

costs: - Area
- Power

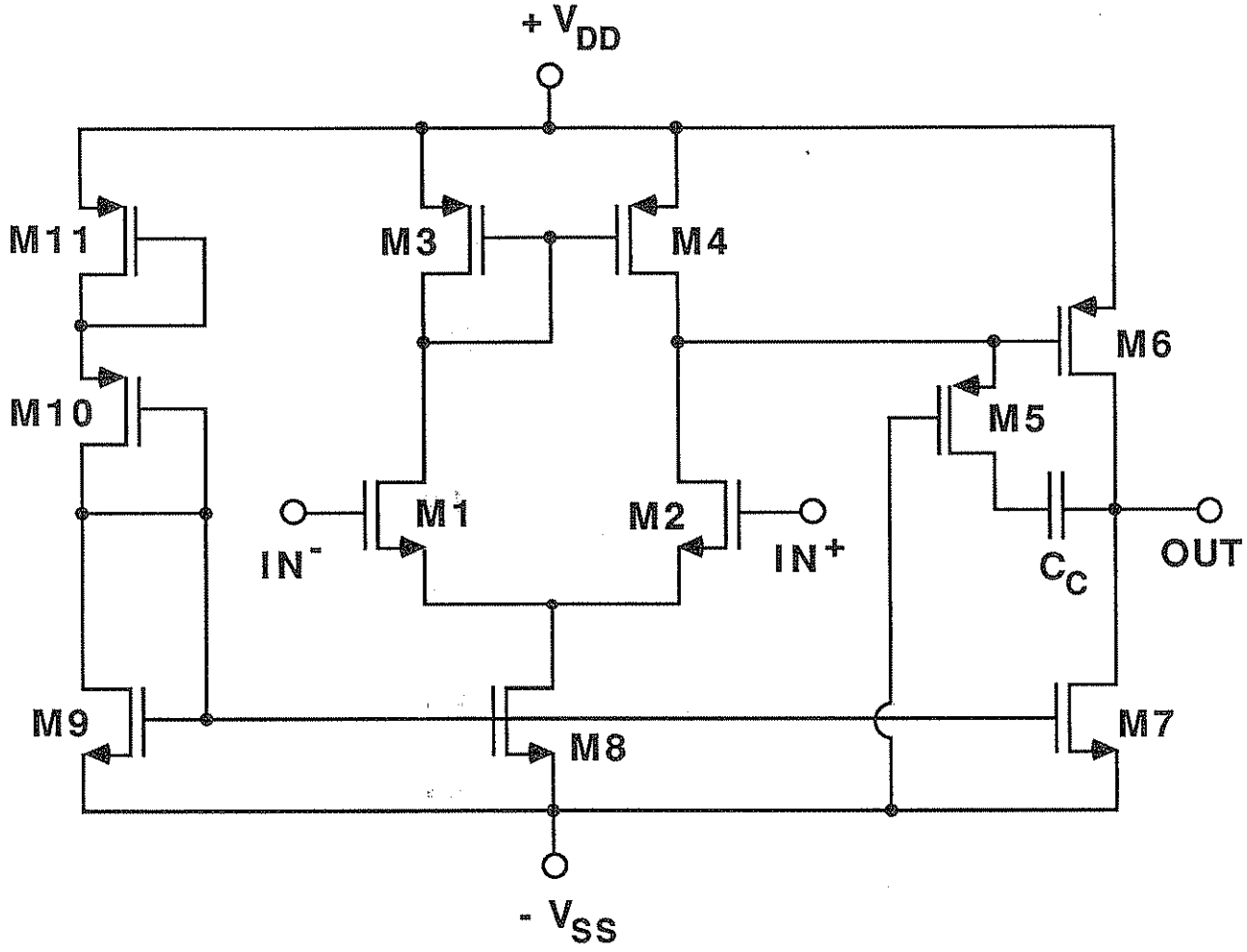
B) with a resistor R_z in the feedback path

zero: $\boxed{\tilde{z}_1' = -\frac{g_m}{C_c(g_m R_z - 1)}}$ g_m: Transcond. of output stage

if $g_m R_z = 1$ zero cancelled
if $g_m R_z > 1$ LHP zero

- consumes no additional power
- requires little additional area

2-Stage CMOS Amplifier



Two-stage Differential Amplifier

By replacing all transistors by their linear equivalent circuits and using first-order analysis techniques, the amplifier differential gain A_d and the common mode rejection ratio CMRR turn out to be:

$$A_d = \frac{g_{m1} r'_{03}\, g_{m6} r'_{06} (1 + sC_c[r_{05} - \frac{1}{g_{m6}}])}{1 + s[C_c r'_{03} g_{m6} r'_{06} + C_L r'_{06}] + s^2 C_c C_L r'_{03}\, r'_{06}}$$

$$CMRR = 2 g_1 r_{08}\, g_{m3}\, r'_{03}$$

where $g_1 = g_{m1} + g_{mb1}$ $r'_{03} = \frac{r_{01} r_{03}}{r_{01} + r_{03}}$ $r'_{06} = \frac{r_{06} r_{07}}{r_{06} + r_{07}}$

The two parameters g_m and g_{bm} denote the transistor gate-source transconductance and body-source (or backgate) transconductance, respectively.

The two poles and the zero that are present in the gain expression are approximately located at:

$$\omega_z = -\frac{g_{m6}}{C_c[g_{m6} r_{05} - 1]}$$

$$\omega_{p1} = -\frac{1}{C_c r'_{03}\, g_{m6} r'_{06}}$$

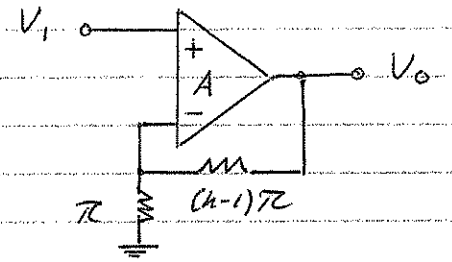
$$\omega_{p2} = -\frac{g_{m6}}{C_L}$$

Note that in order to guarantee a left half-plane zero, the product $g_{m6} r_{05}$ has to be greater than 1.

Most often, the nondominant second pole and the zero of the amplifier are kept equal to or greater than the unity-gain frequency GB. The frequency response can then be modeled by a first-order lowpass circuit. The unity-gain frequency is then approximately equal to:

$$GB = |A_d\, \omega_{p1}| = \frac{g_{m1}}{C_c}$$

Amplifier in Feedback Configuration



$$V_o = \left(V_i - \frac{V_o}{k}\right) \cdot A \qquad k \geq 1$$

$$\left\| \frac{V_o}{V_i} = \frac{A}{\left(1 + \frac{A}{k}\right)} \right\|$$

$$\left| A(s) = \frac{A_0}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)\left(1 + \frac{s}{p_3}\right)} \right| \qquad p_1, p_2 \text{ \& } p_3 \text{ are neg. real poles}$$

- Is this circuit stable for all possible values of k?
- Find poles of closed loop system as a function of feedback parameter k

$$\left| \frac{V_o(s)}{V_i(s)} = \frac{A_0}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)\left(1 + \frac{s}{p_3}\right) + \frac{A_0}{k}} \right|$$

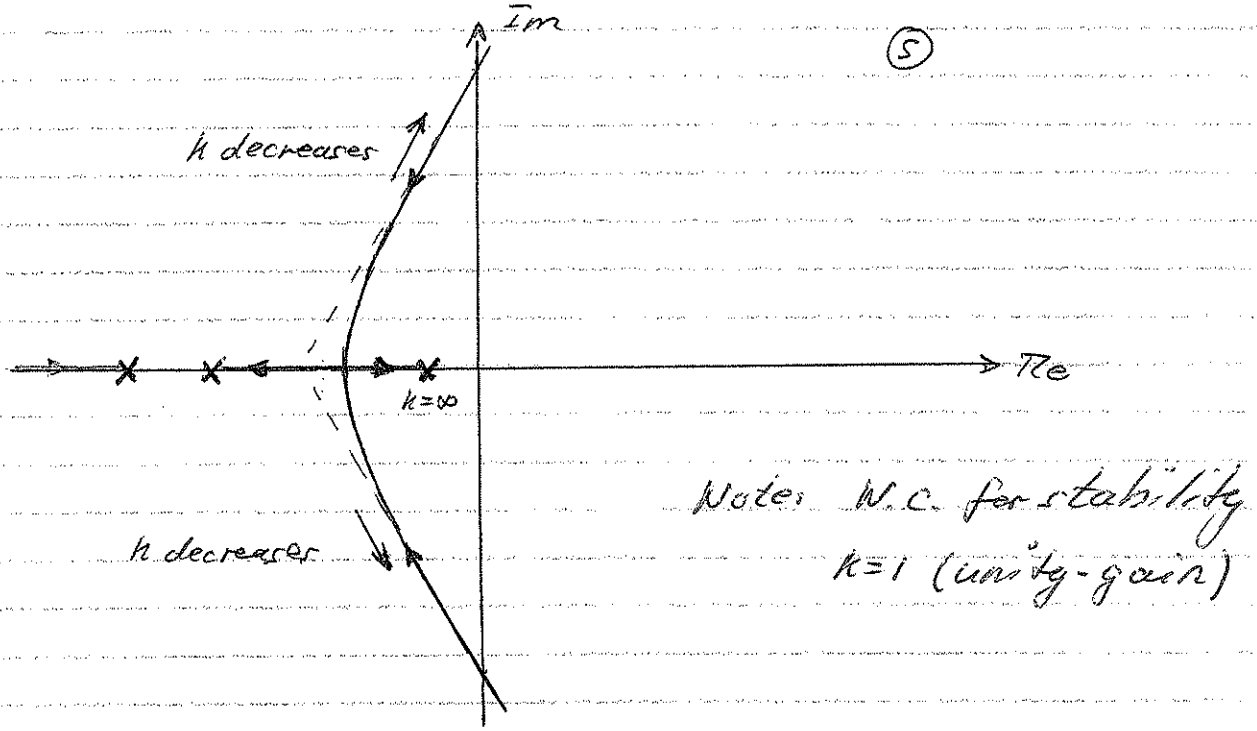
- Find Root Locus plot for the 3 poles as a function of k

characteristic equation of closed-loop system

$$\left\| D(s) = 1 + \frac{k}{A_0}\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)\left(1 + \frac{s}{p_3}\right) \right\| \qquad 1 \leq k < A_0$$

$$\left| D(s) = 1 + \mu \cdot L(s) \right| \qquad \mu = \frac{k}{A_0} \qquad \frac{1}{A_0} \leq \mu < 1$$

Root Locus Plot for 3 neg. real poles in open-loop



Note: N.C. for stability
$k=1$ (unity-gain)

Conclusion:

Depending on the initial position of the open-loop poles, the closed-loop system can become unstable as k approaches 1

Note:

If initial poles are closely spaced, the system is very likely to become unstable in a closed-loop configuration

Solution: Split poles apart

$p_2 \approx 10 p_1 \quad p_3 > p_2$

Opamp Stability Analysis

Pole/zero locations as a function of Phase Compensation Circuitry

g_{ms}: Source Follower Transcond.

pole/zero	uncomp.	C_c+R_c	Source Follower
ω_z	∞	$-\frac{g_{m2}}{C_c[g_{m2}R_c - 1]}$	$-\frac{g_{ms}}{C_c}$
ω_{p1}	$-\frac{1}{r_{o1}C_1}$	$-\frac{1}{r_{o1}C_c g_{m2} r_{o2}}$	$-\frac{1}{r_{o1}C_c g_{m2} r_{o2}}$
ω_{p2}	$-\frac{1}{r_{o2}C_2}$	$-\frac{g_{m2}}{C_2[1+\frac{C_1}{C_c}+\frac{C_1}{C_2}]}$	$-\frac{g_{m2}}{C_2[1+\frac{C_1}{C_c}+\frac{C_1}{C_2}]}$

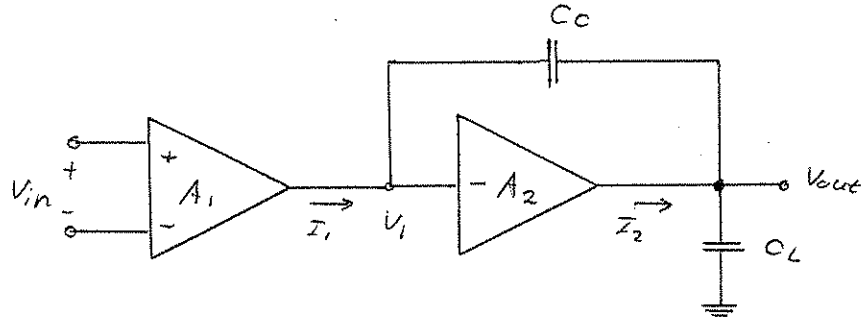
Numerical Example

$g_{m2} = 500\mu S$ $\quad g_{ms} = 100\mu S$ $\quad R_c = 12k\Omega$ $\quad r_{o1} = 500k\Omega$

$r_{o2} = 200k\Omega$ $\quad C_1 = 200fF$ $\quad C_2 = 5pF$ $\quad C_c = 2pF$

pole/zero	uncomp.	C_c+R_c	Source Follower
ω_z	∞	-50×10^6	-50×10^6
ω_{p1}	-10×10^6	-10×10^3	-10×10^3
ω_{p2}	-1.0×10^6	-87.7×10^6	-87.7×10^6
ω_{p3}	∞	-417×10^6	-500×10^6

4. Slew Rate



Note:
since $|A_2| \gg 1$
$\therefore V_1 \cong 0$

Slew Rate limit:

$$SR = \left.\frac{dV_{out}}{dt}\right|_{Max} = Min\left\{\frac{I_{1Max}}{C_c}\ ;\ \frac{I_{2Max}}{(C_c+C_L)}\right\}$$

Note: $I_{1Max} = I_{diff}$ $\quad I_{2Max} = I_{out}$ (for class A output stage)

If $SR_1 = SR_2$ $\quad\therefore\quad \frac{I_{diff}}{C_c} = \frac{I_{out}}{C_c+C_L}$ $\quad$ or $I_{out} = I_{diff}\left(1+\frac{C_L}{C_c}\right)$

If second pole of amplifier is at the unity-gain frequency, then $\boxed{|GB \cong \frac{g_{m1}}{C_c}|}$

Furthermore if $SR = SR_1 = \frac{I_{diff}}{C_c}$

then $SR = GB\,\frac{I_{diff}}{g_{m1}}$

since $g_{m1} = \sqrt{\mu C_{ox}\left(\frac{W}{L}\right)_1 \cdot \frac{1}{2} I_{diff} \cdot 2}$

we obtain $\boxed{SR \cong GB\sqrt{\frac{I_{diff}}{\mu C_{ox}\left(\frac{W}{L}\right)_1}}}$

Performance Criteria and Design Guidlines

1. Gain
   - o low bias current
   - o long devices → high r_o
   - o wide devices → high g_m
   - o cascode configuration

2. Bandwidth ($BW \propto \frac{g_m}{C}$)
   - o high bias current
   - o short channels

3. Slew Rate
   - o high bias current

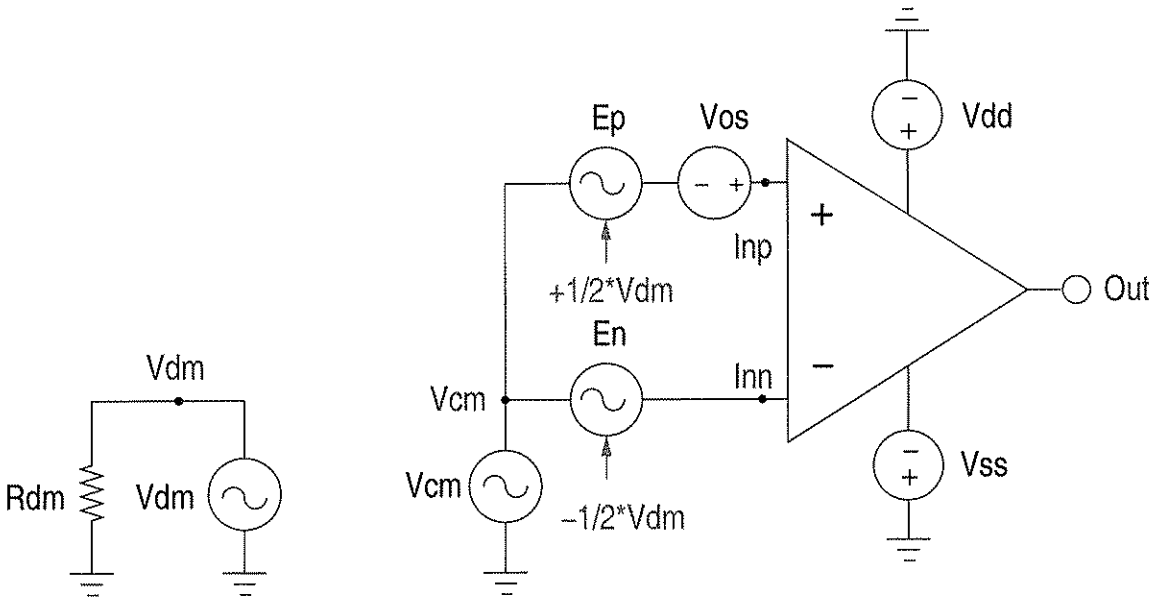
4. Offset Voltage
   - o large devices
   - o low bias current → small V_{eff}

5. Noise
   - o large devices → less 1/f noise
   - o high bias → high g_m

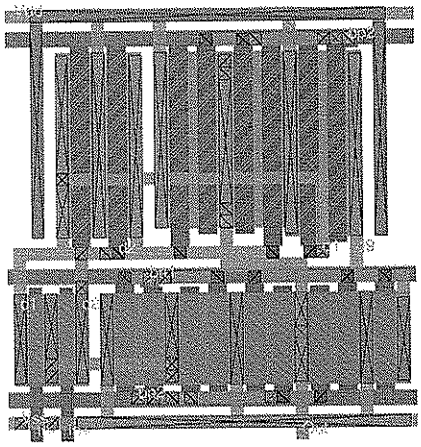
Good Design = Good Compromize among conflicting criteria

OpAmp Performance Evaluation

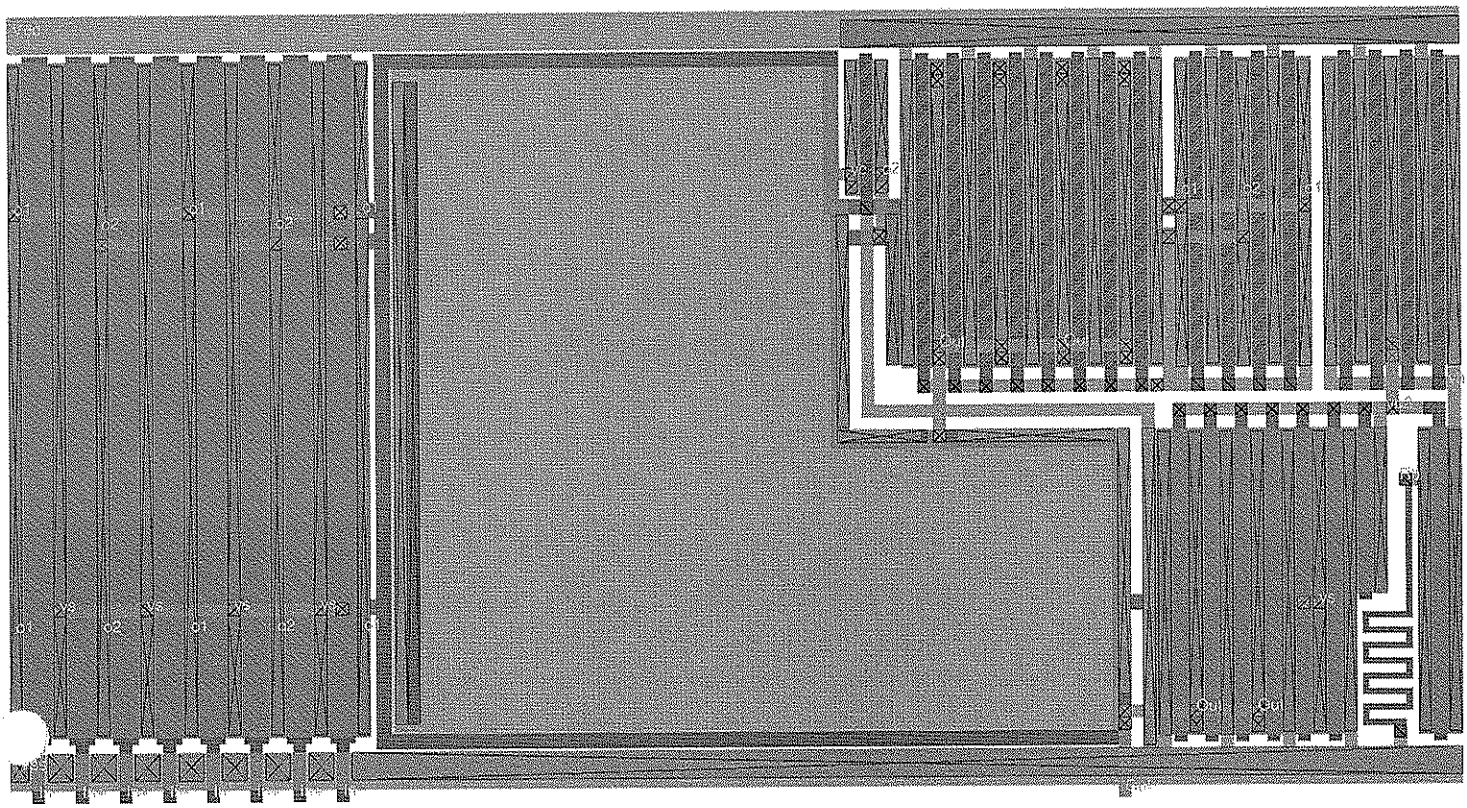
Test Circuit Set–up for Spice



0.5μm CMOS OPAMPS



40μm

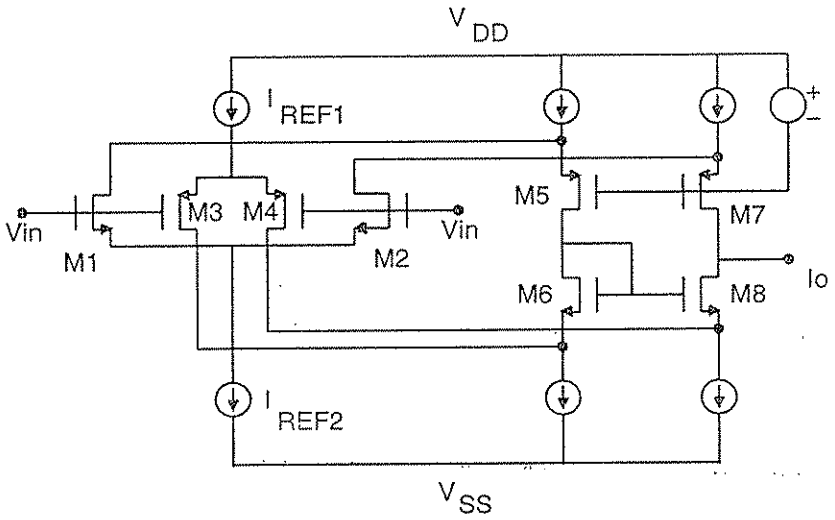


Low-Voltage Amplifiers

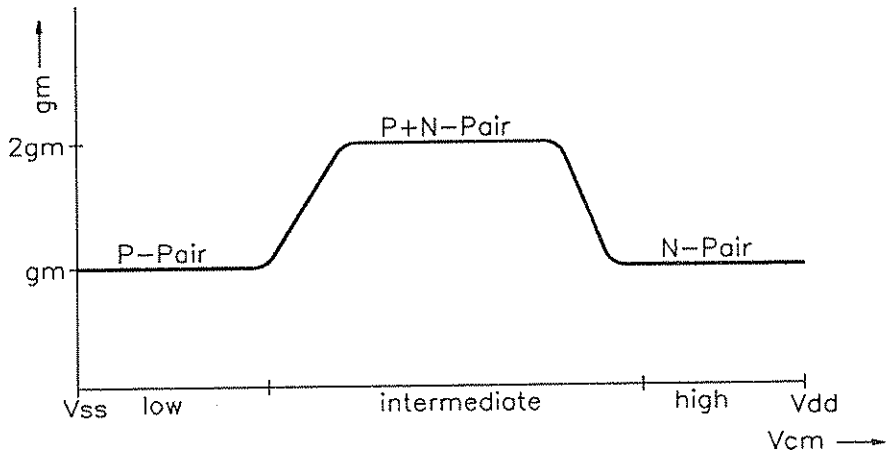
In order to keep the signal-to-offset, and signal-to-noise ratio as large as possible, circuits must be designed which have rail-to-rail input and output voltage swing.

A) Input stage with Rail-to-Rail Swing

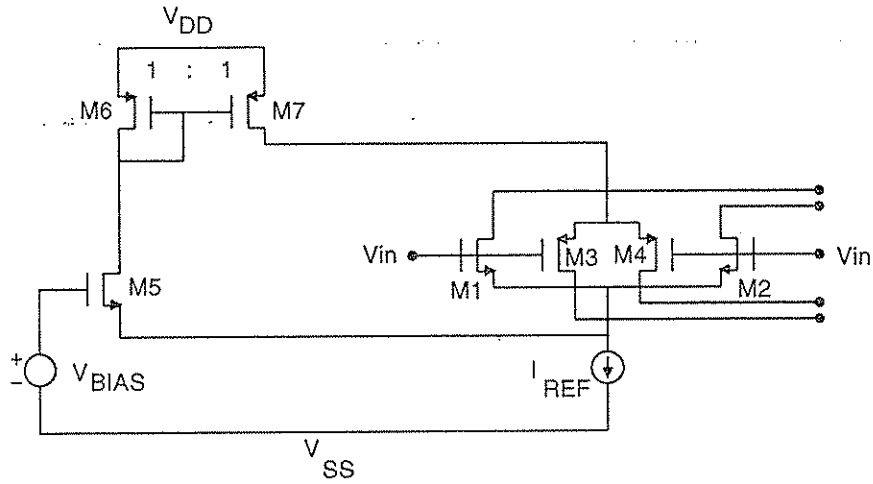
Basic configuration



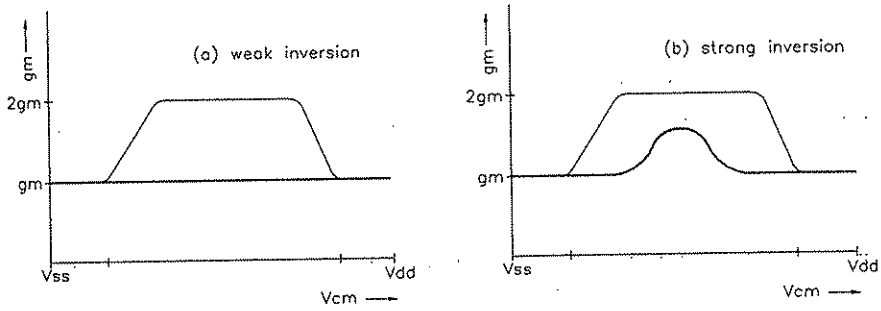
Problem: Transconductance of input stage varies as v_{cm} is changed



Solution: keep total diff. input current constant



Resulting input transconductance

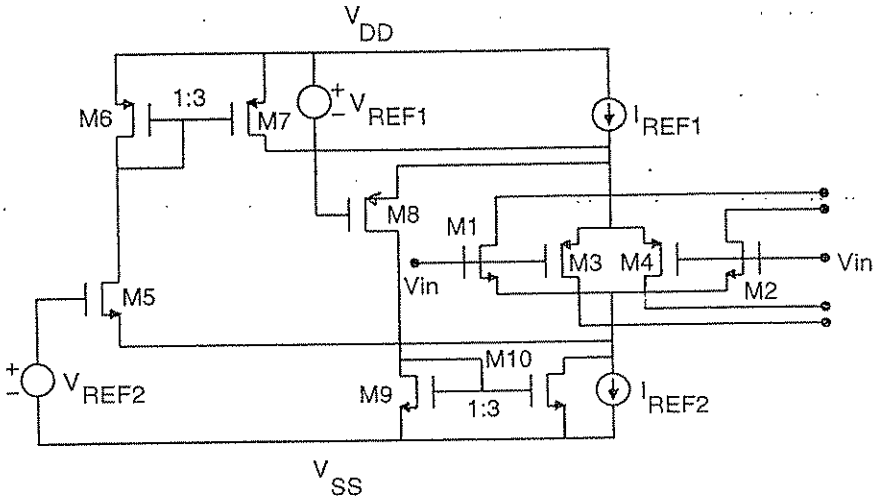


Comment: This solution works fine if the input stages are operated in weak inversion where the transconductance is proportional to the bias current. For the more typical case, however, where the input stages are operated in strong inversion (i.e. saturation), a 40% deviation results since

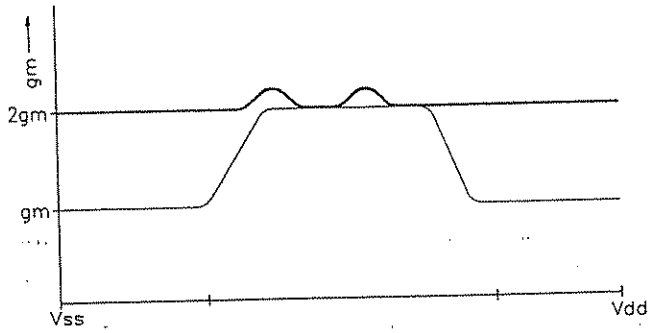
$$G_{m_{sat}} \propto \left[\sqrt{I_0 \cdot x} + \sqrt{I_0 (1-x)} \right]$$

where $\text{Max}\left[\sqrt{I_0 x} + \sqrt{I_0 (1-x)} \right] = 1.41 \cdot \sqrt{I_0}$

Improved Solution

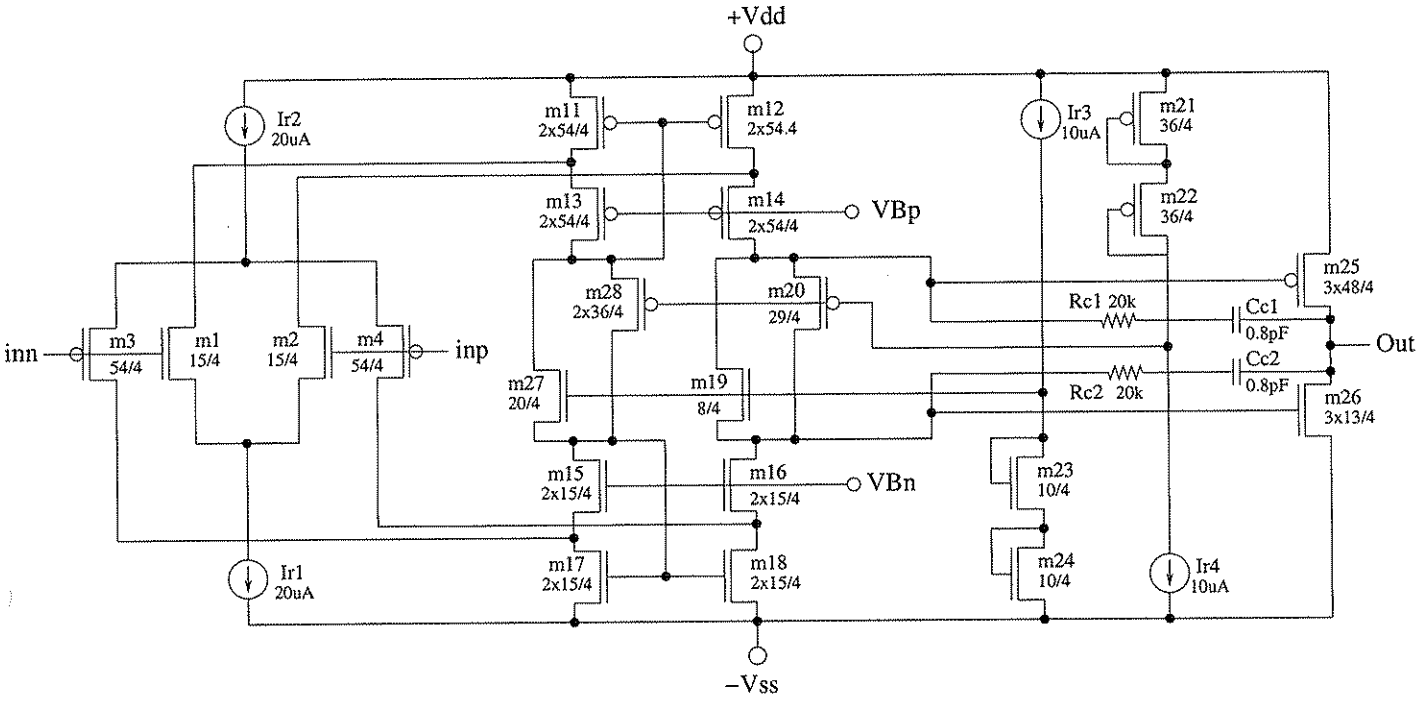


Resulting Transconductance (per saturation)

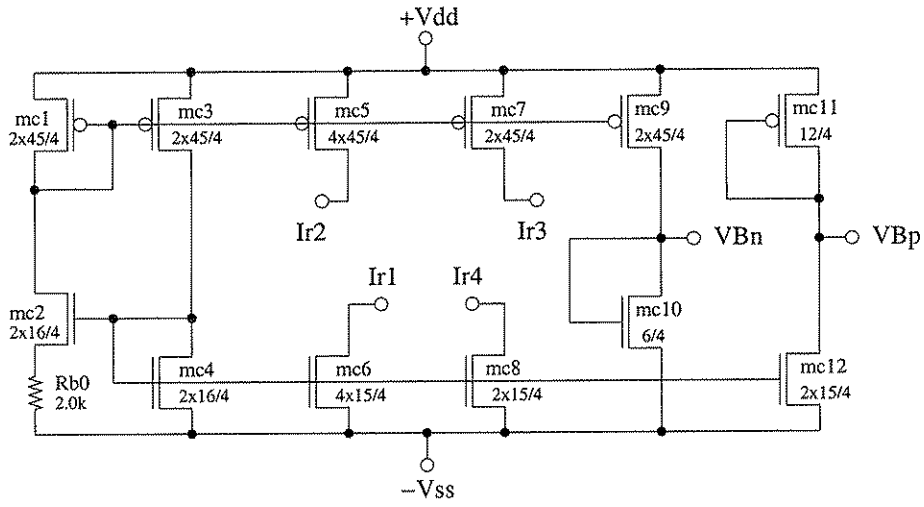


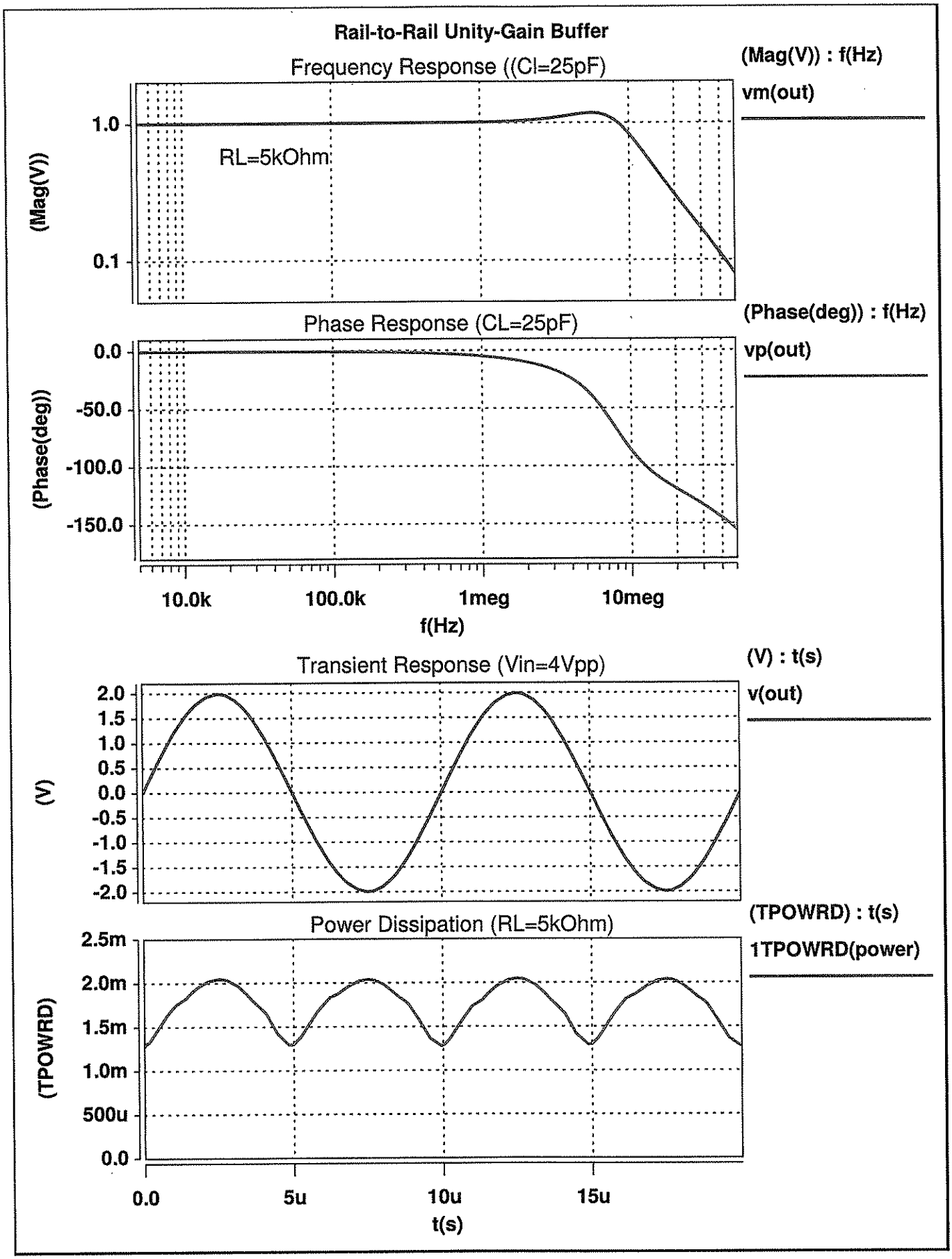
CMOS Amplifier with Rail–to–Rail Common–Mode Input Range

Core Amplifier Circuit



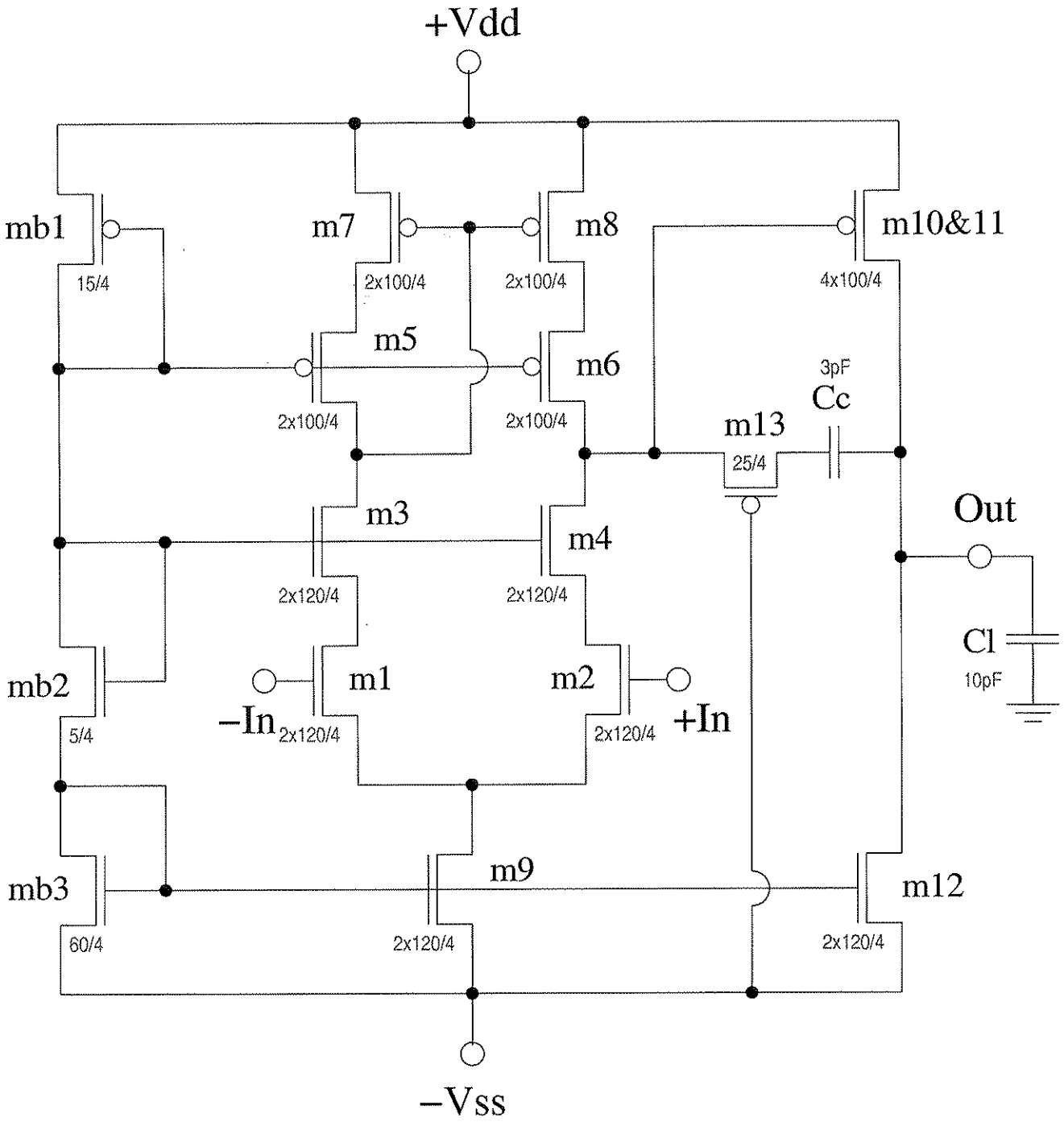
Bias Circuitry

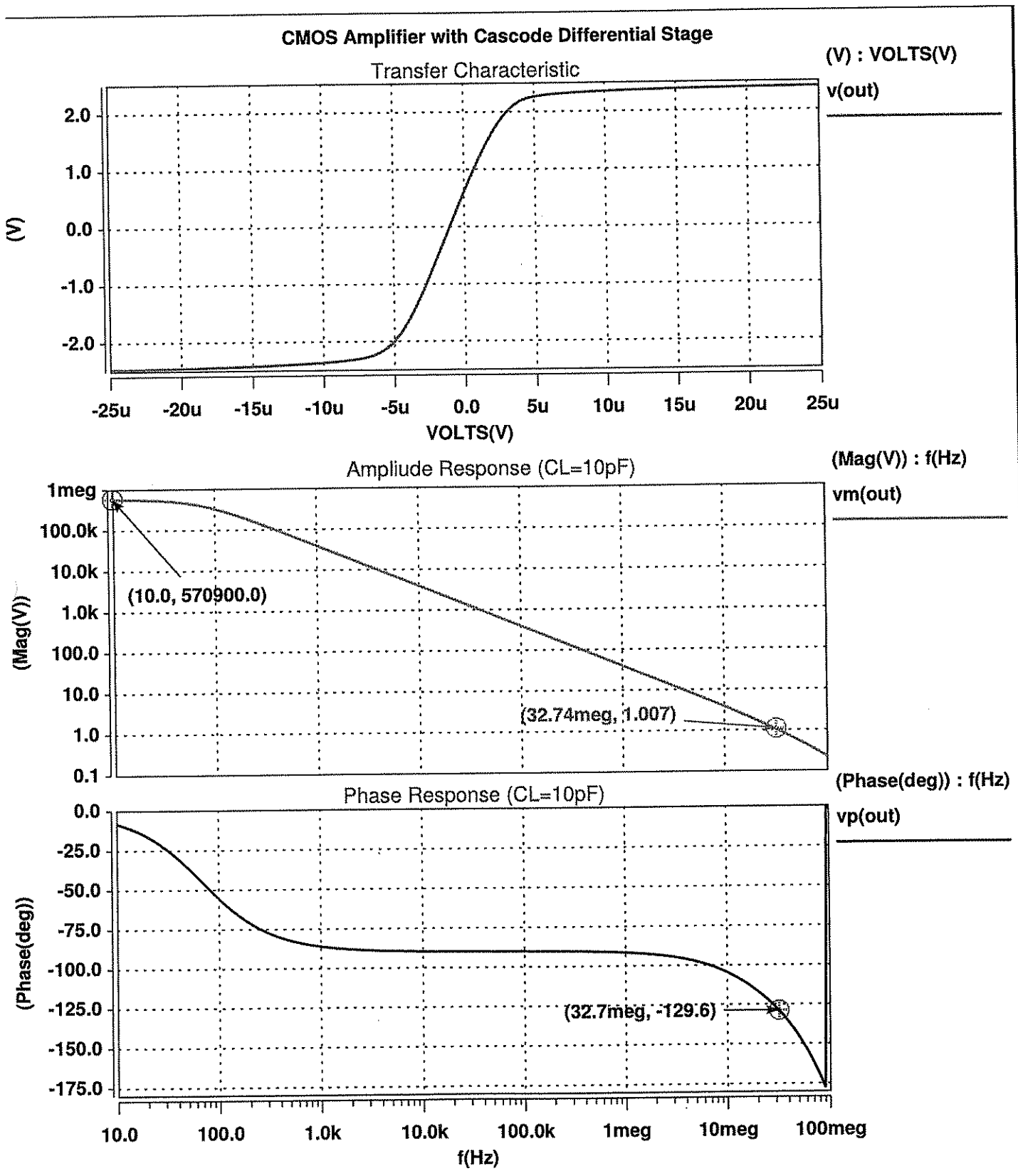



Rail-to-Rail Unity-Gain Buffer
Frequency Response ((Cl=25pF)
(Mag(V)) : f(Hz)
vm(out)
1.0
0.1
(Mag(V))
RL=5kOhm
Phase Response (CL=25pF)
(Phase(deg)) : f(Hz)
vp(out)
0.0
-50.0
-100.0
-150.0
(Phase(deg))
10.0k
100.0k
1meg
10meg
f(Hz)
Transient Response (Vin=4Vpp)
(V) : t(s)
v(out)
2.0
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
(V)
Power Dissipation (RL=5kOhm)
(TPOWRD) : t(s)
1TPOWRD(power)
2.5m
2.0m
1.5m
1.0m
500u
0.0
(TPOWRD)
0.0
5u
10u
15u
t(s)

High Gain CMOS Opamp with Cascode Input Stage

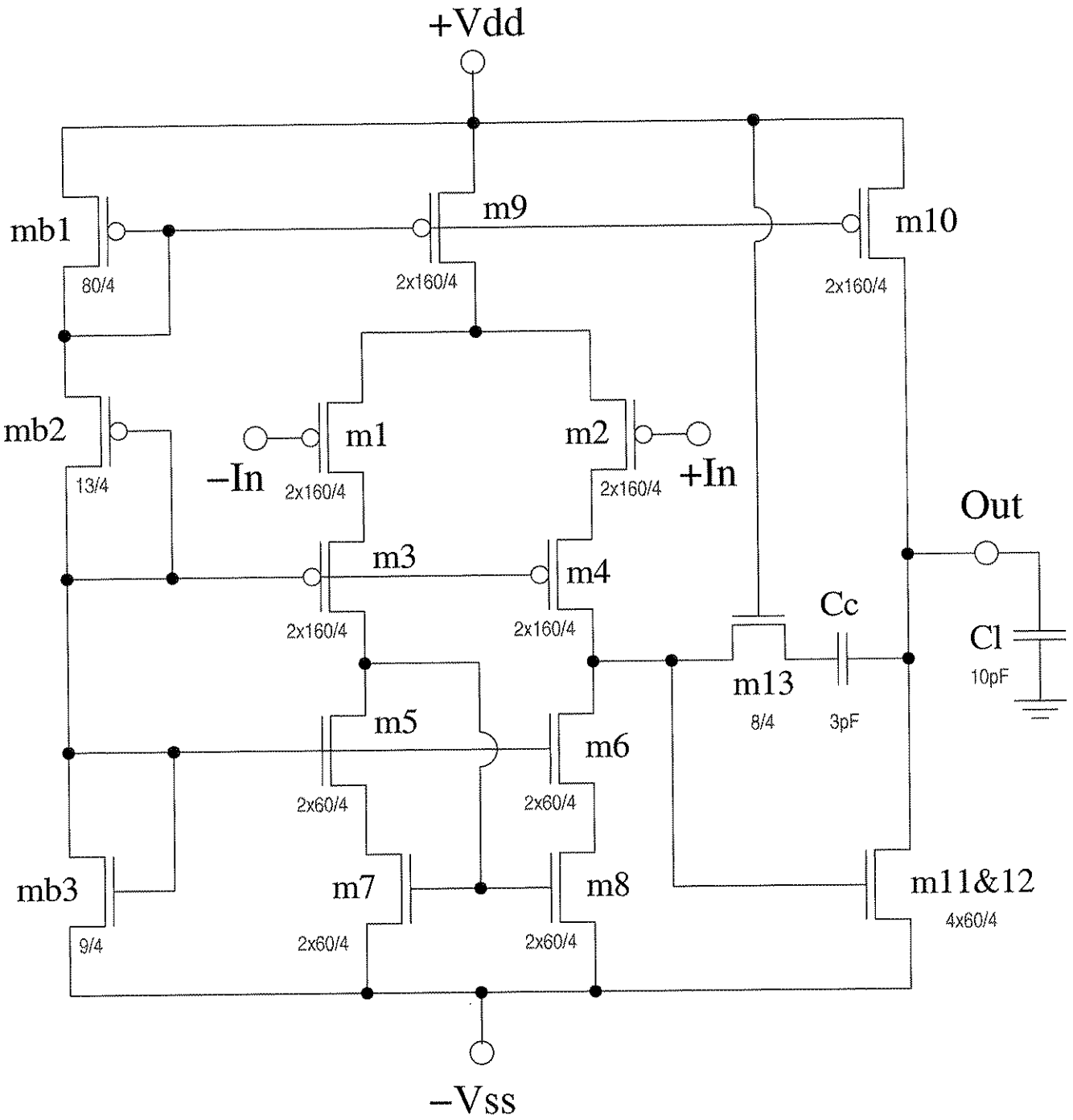
Version 1 with n–channel Input Pair



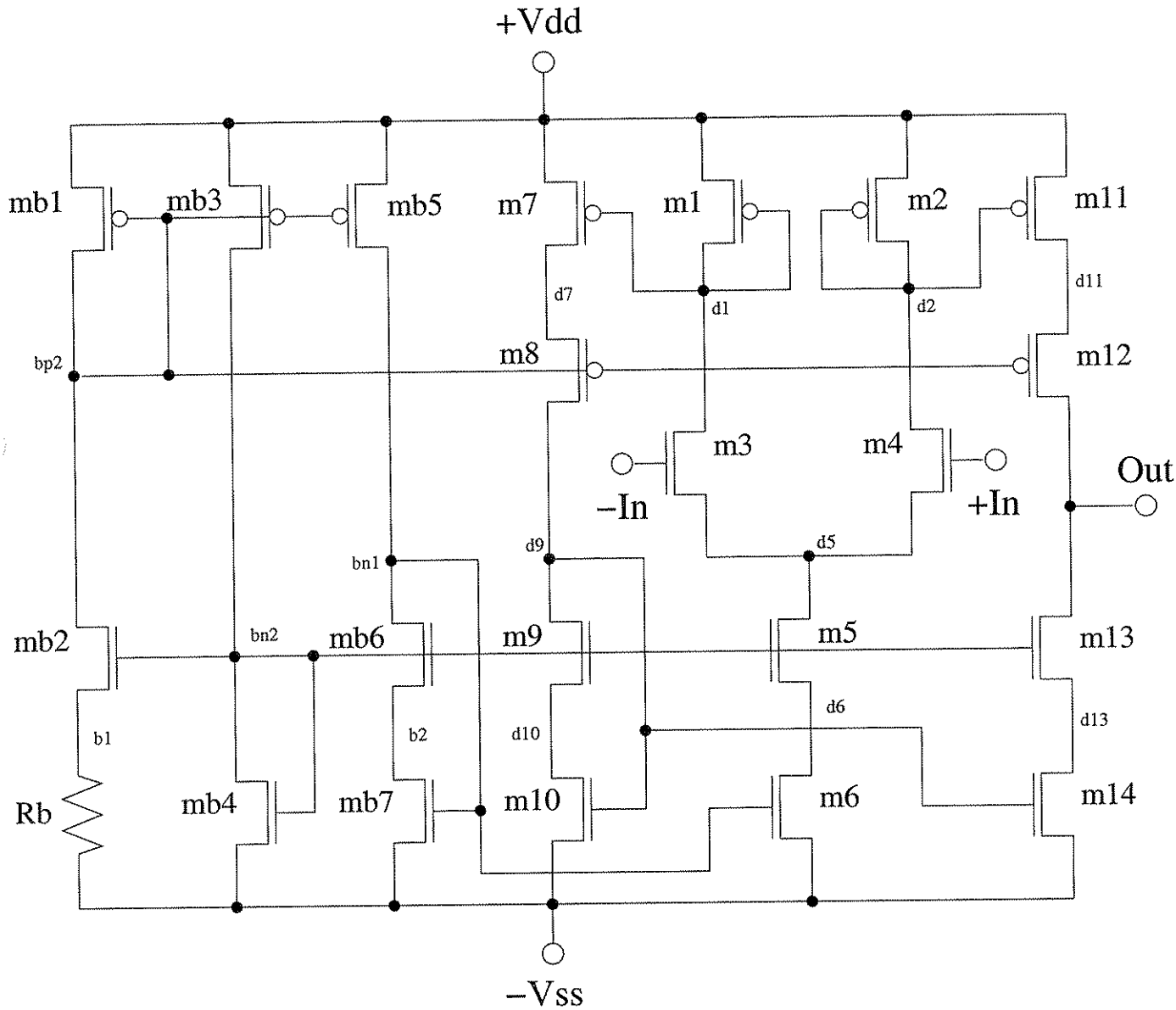

CMOS Amplifier with Cascode Differential Stage
Transfer Characteristic
(V) : VOLTS(V)
v(out)
(V)
2.0
1.0
0.0
-1.0
-2.0
-25u
-20u
-15u
-10u
-5u
0.0
5u
10u
15u
20u
25u
VOLTS(V)
Ampliude Response (CL=10pF)
(Mag(V)) : f(Hz)
vm(out)
(Mag(V))
1meg
100.0k
10.0k
1.0k
100.0
10.0
1.0
0.1
(10.0, 570900.0)
(32.74meg, 1.007)
Phase Response (CL=10pF)
(Phase(deg)) : f(Hz)
vp(out)
(Phase(deg))
0.0
-25.0
-50.0
-75.0
-100.0
-125.0
-150.0
-175.0
(32.7meg, -129.6)
10.0
100.0
1.0k
10.0k
100.0k
1meg
10meg
100meg
f(Hz)

High Gain CMOS Opamp with Cascode Input Stage

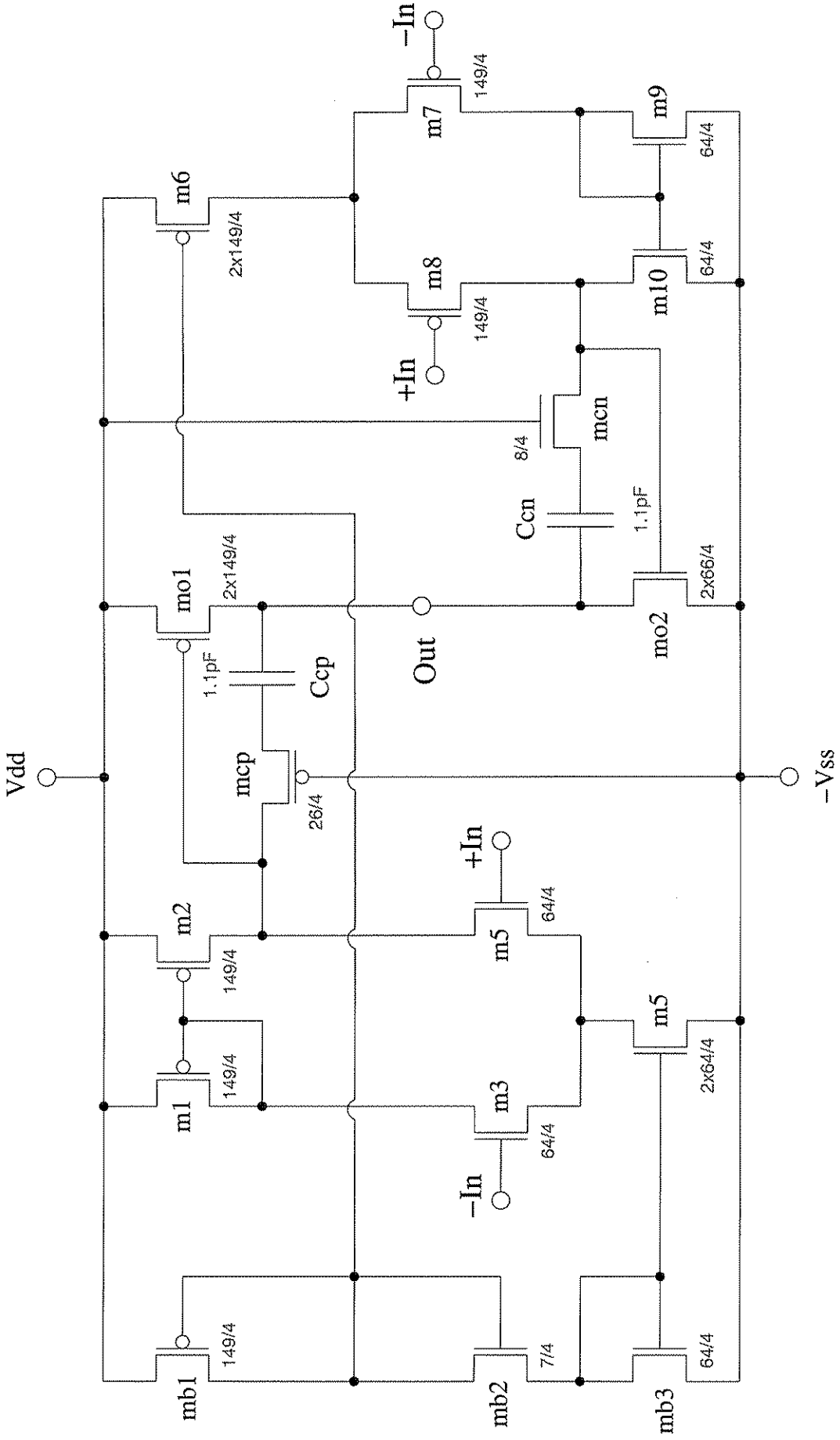
Version2 with p–channel Input Pair

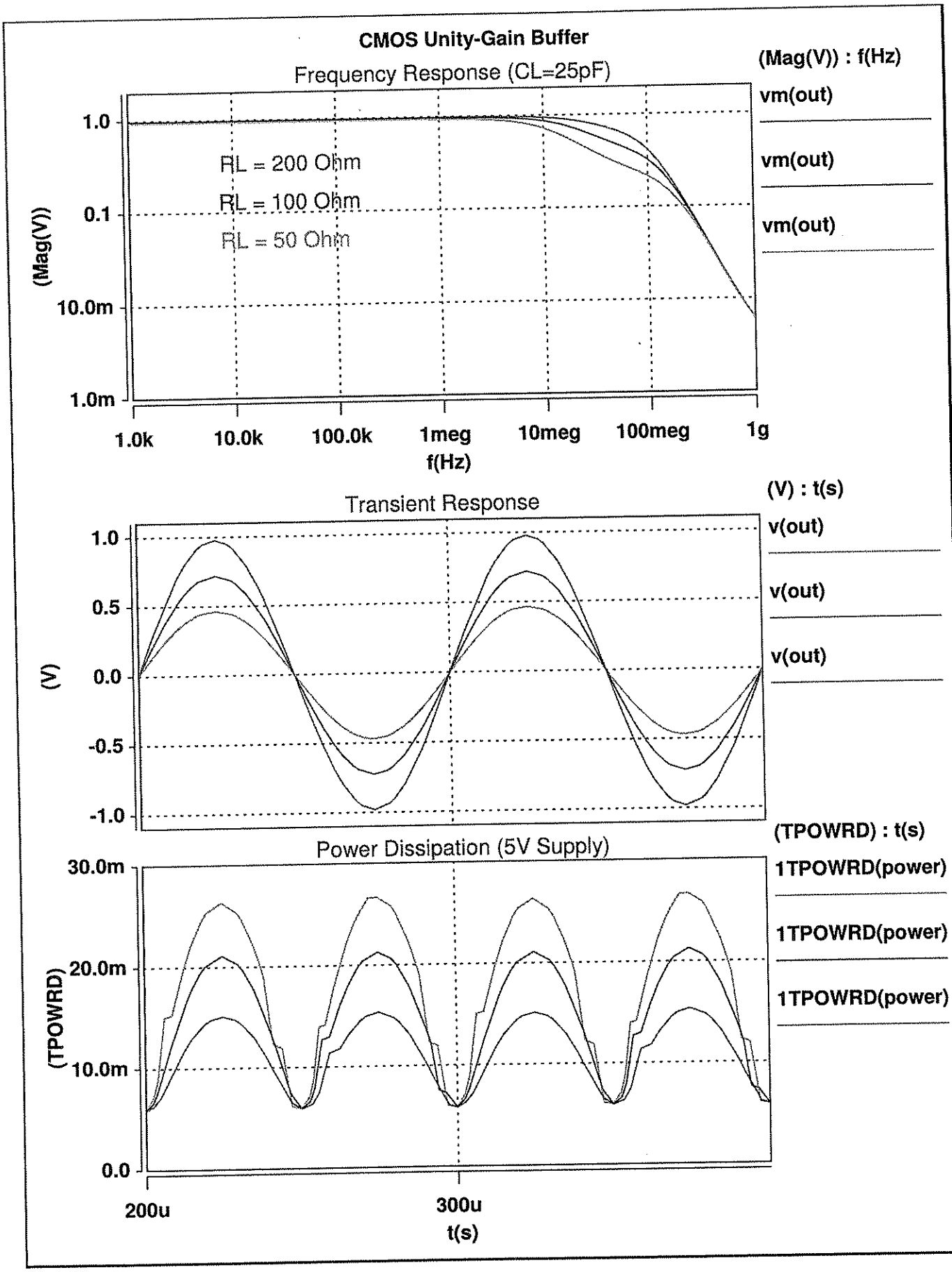


CMOS Transconductance Amplifier

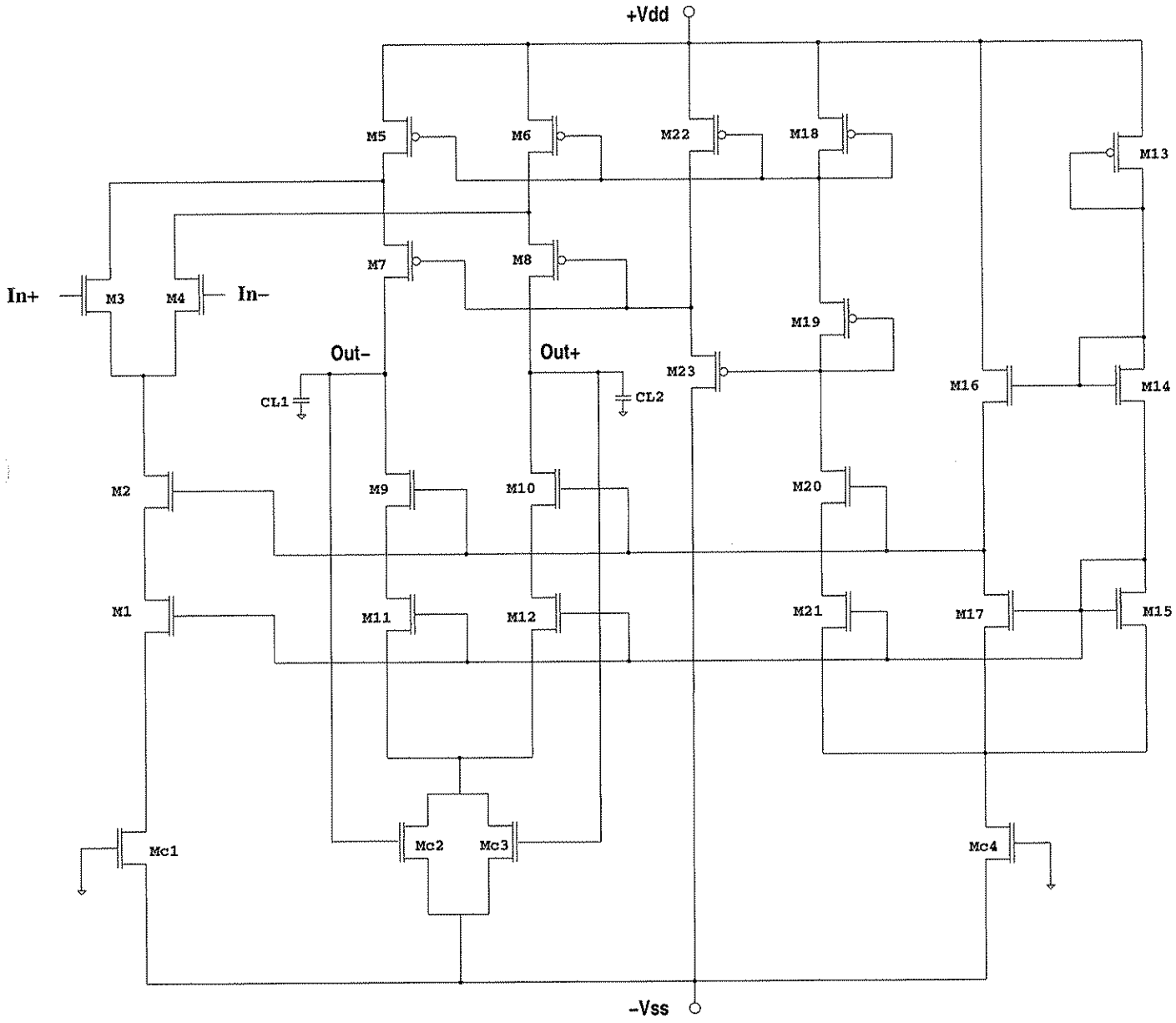


CMOS Push–Pull Amplifier with high Current Driving Capability

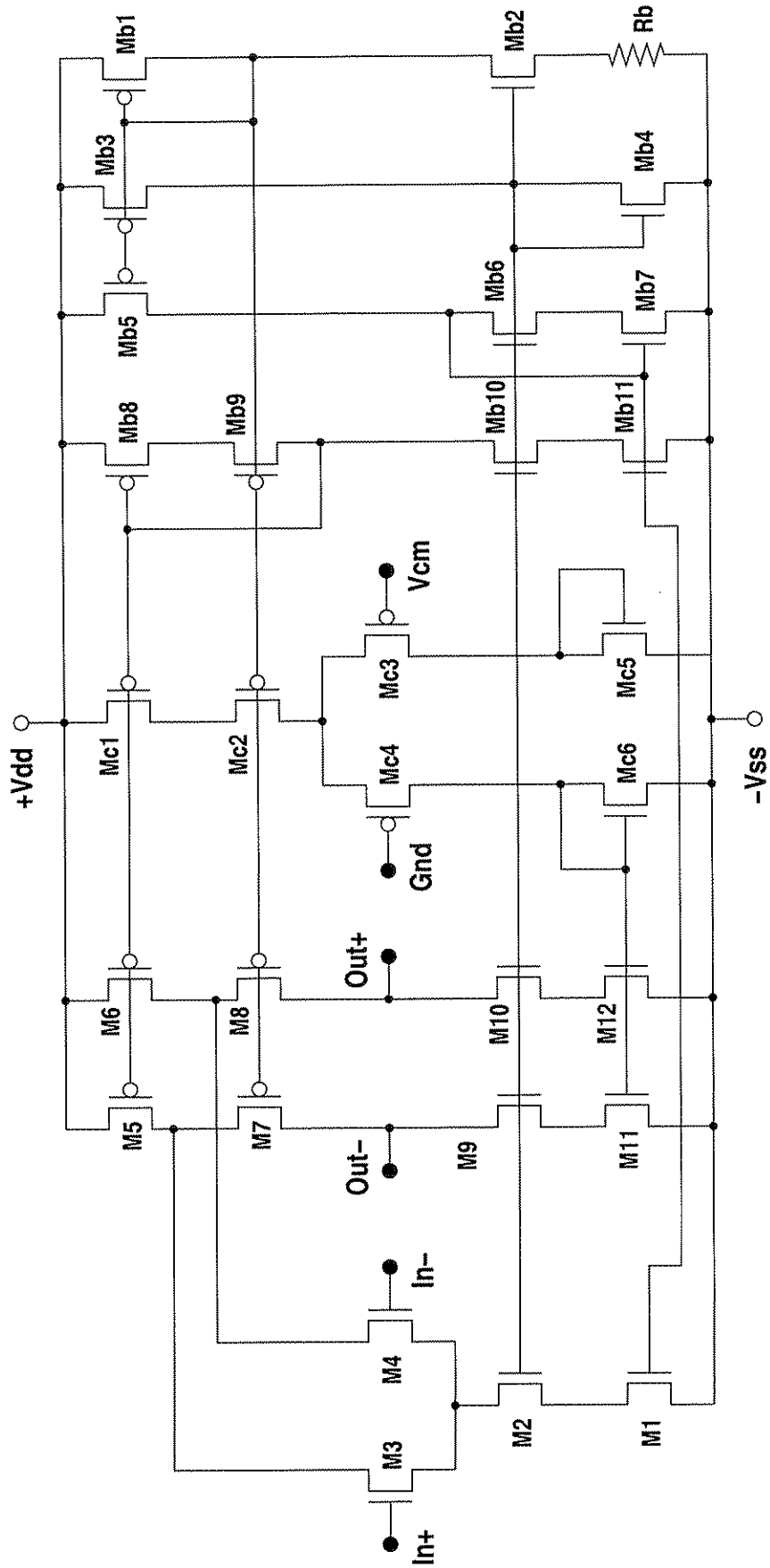


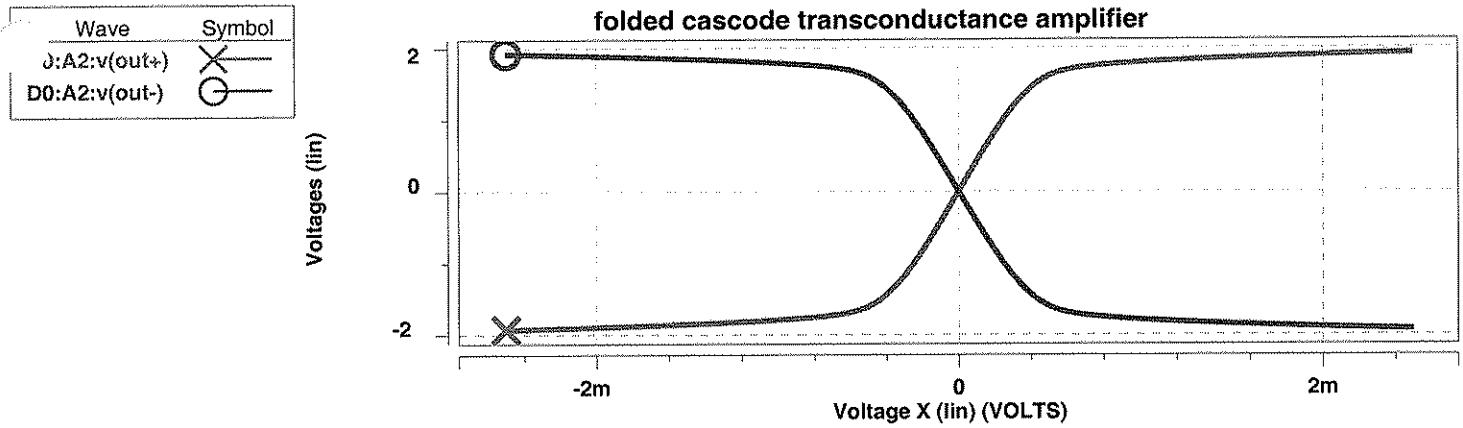

CMOS Unity-Gain Buffer
Frequency Response (CL=25pF)
(Mag(V)) : f(Hz)
vm(out)
vm(out)
vm(out)
RL = 200 Ohm
RL = 100 Ohm
RL = 50 Ohm
1.0
0.1
10.0m
1.0m
(Mag(V))
1.0k
10.0k
100.0k
1meg
10meg
100meg
1g
f(Hz)
Transient Response
(V) : t(s)
v(out)
v(out)
v(out)
1.0
0.5
0.0
-0.5
-1.0
(V)
Power Dissipation (5V Supply)
(TPOWRD) : t(s)
1TPOWRD(power)
1TPOWRD(power)
1TPOWRD(power)
30.0m
20.0m
10.0m
0.0
(TPOWRD)
200u
300u
t(s)

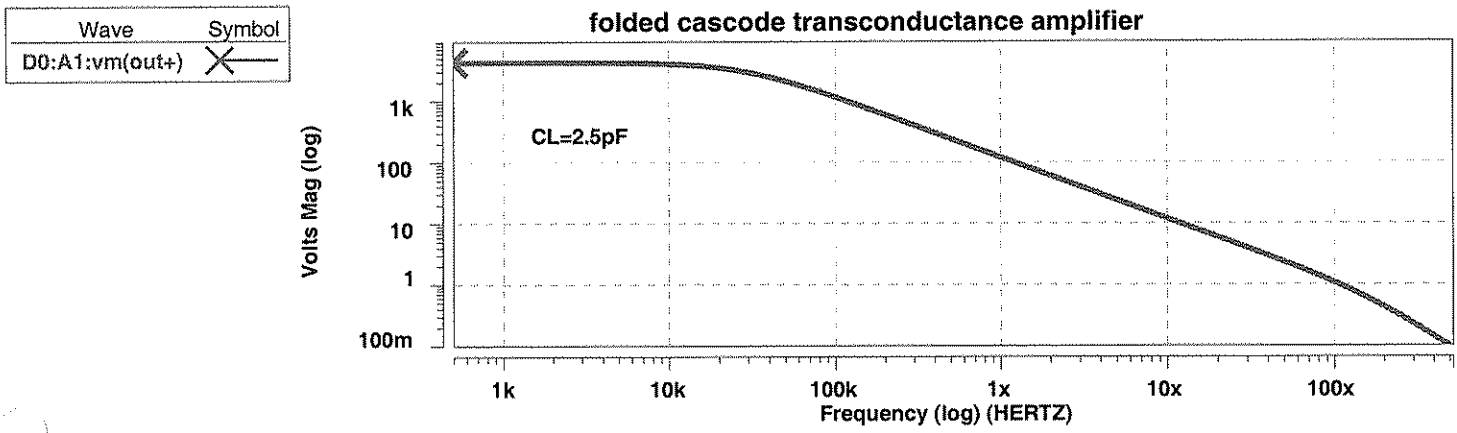
Folded Cascode Transconductance Amplifier with passive Common Mode Feedback

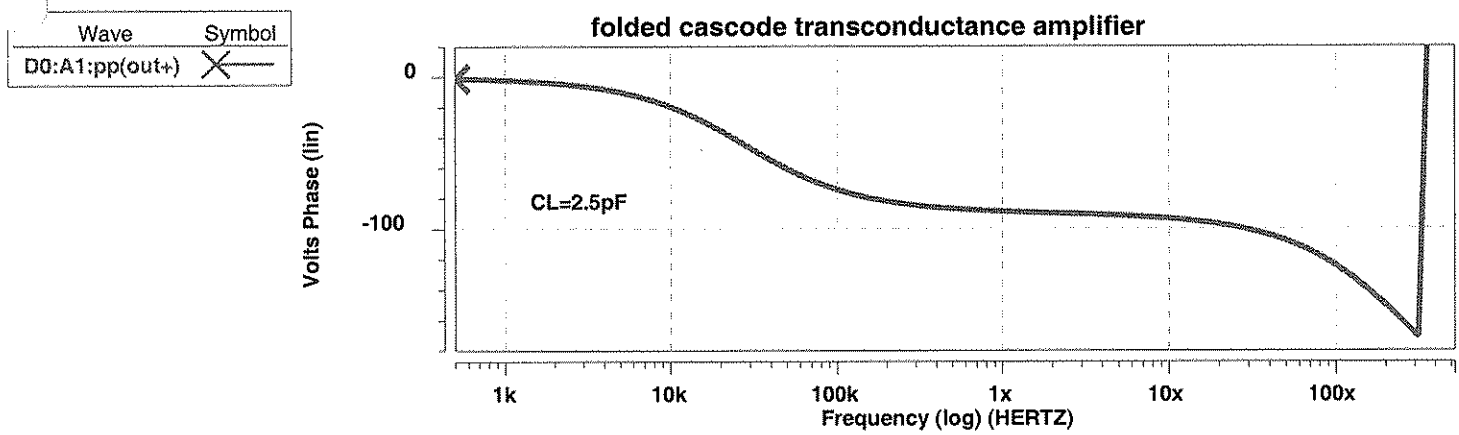


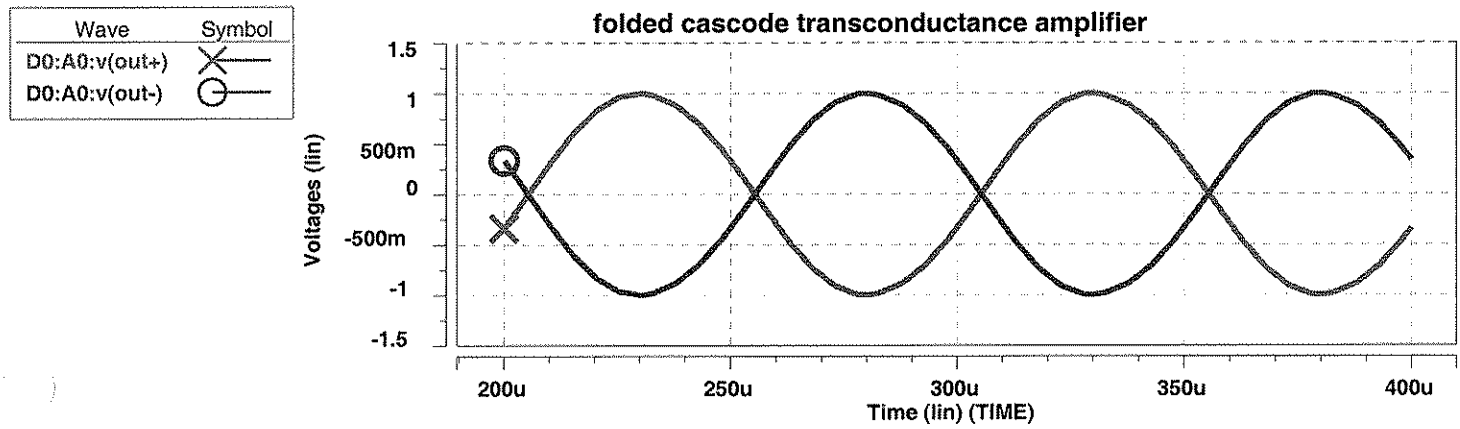
Folded Cascode Fully–Differential Transconductance Amplifier with active CMF




Wave
Symbol
♪:A2:v(out+)
D0:A2:v(out-)
folded cascode transconductance amplifier
Voltages (lin)
2
0
-2
-2m
0
2m
Voltage X (lin) (VOLTS)

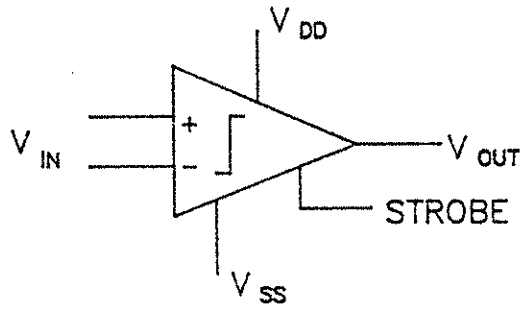

Wave
Symbol
D0:A1:vm(out+)
folded cascode transconductance amplifier
Volts Mag (log)
1k
100
10
1
100m
CL=2.5pF
1k
10k
100k
1x
10x
100x
Frequency (log) (HERTZ)

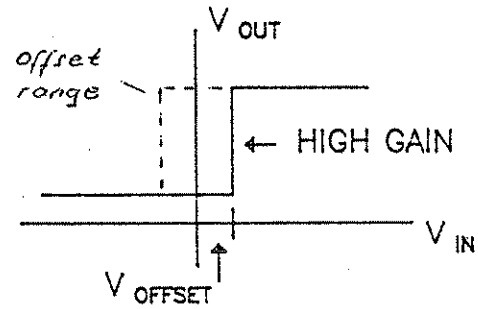

Wave
Symbol
D0:A1:pp(out+)
folded cascode transconductance amplifier
Volts Phase (lin)
0
-100
CL=2.5pF
1k
10k
100k
1x
10x
100x
Frequency (log) (HERTZ)


Wave
Symbol
D0:A0:v(out+)
D0:A0:v(out-)
folded cascode transconductance amplifier
Voltages (lin)
1.5
1
500m
0
-500m
-1
-1.5
200u
250u
300u
350u
400u
Time (lin) (TIME)

COMPARATORS

A. Definition and Features

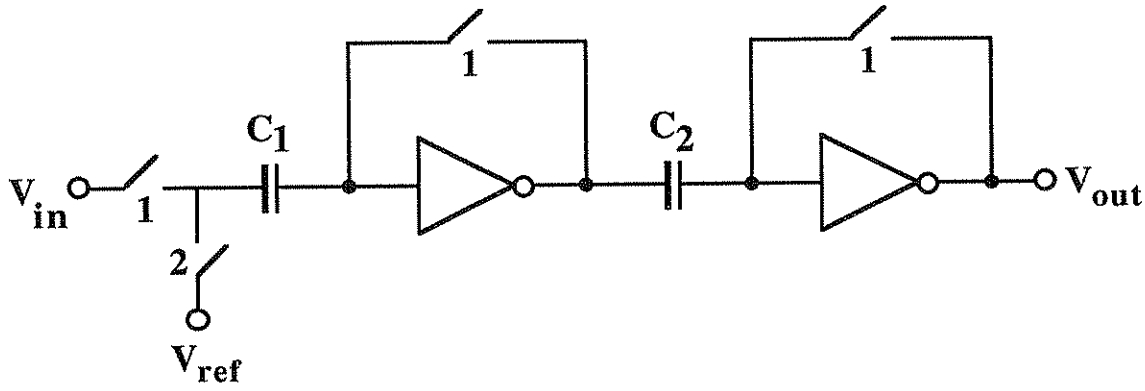




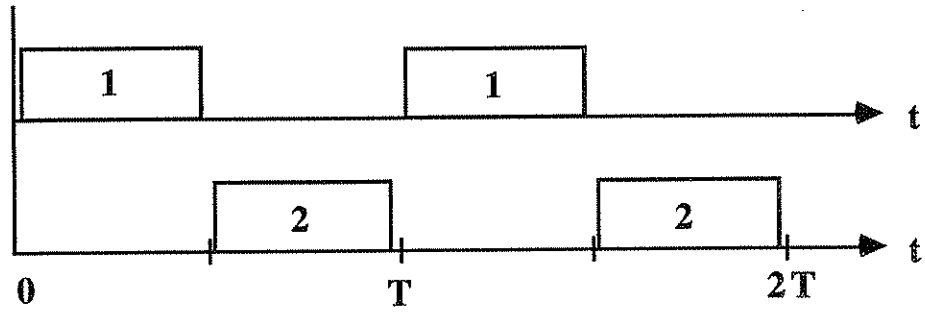
B. Requirements

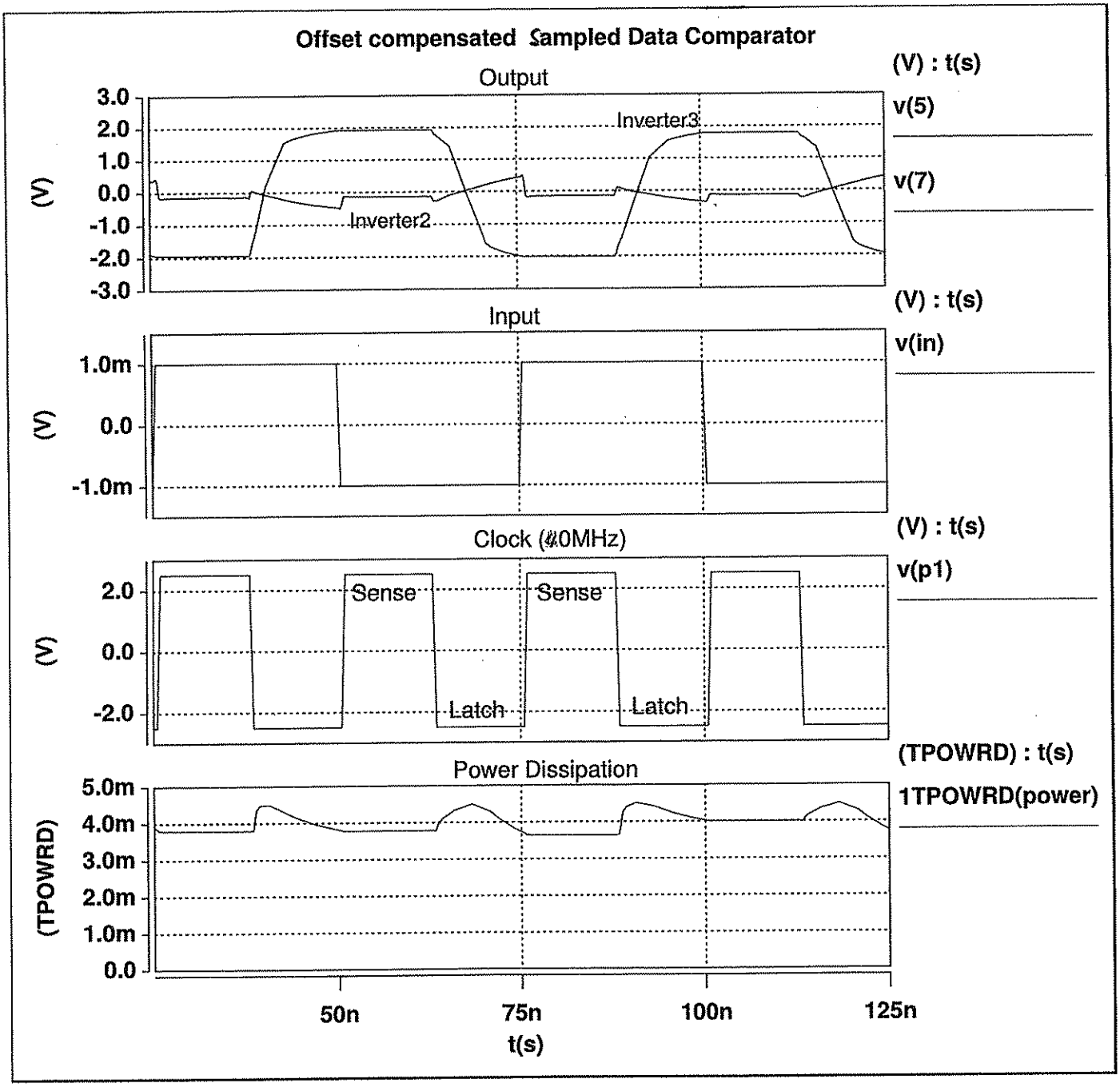
1. HIGH GAIN 10K *Alternative: Employ positive feedback*
2. LOW OFFSET VOLTAGE
3. COMMON MODE REJECTION ≈ 40dB
4. FAST RESPONSE < 1μsec
5. LOW POWER; SMALL AREA
6. STROBE

Sampled-Data Comparator Version 1

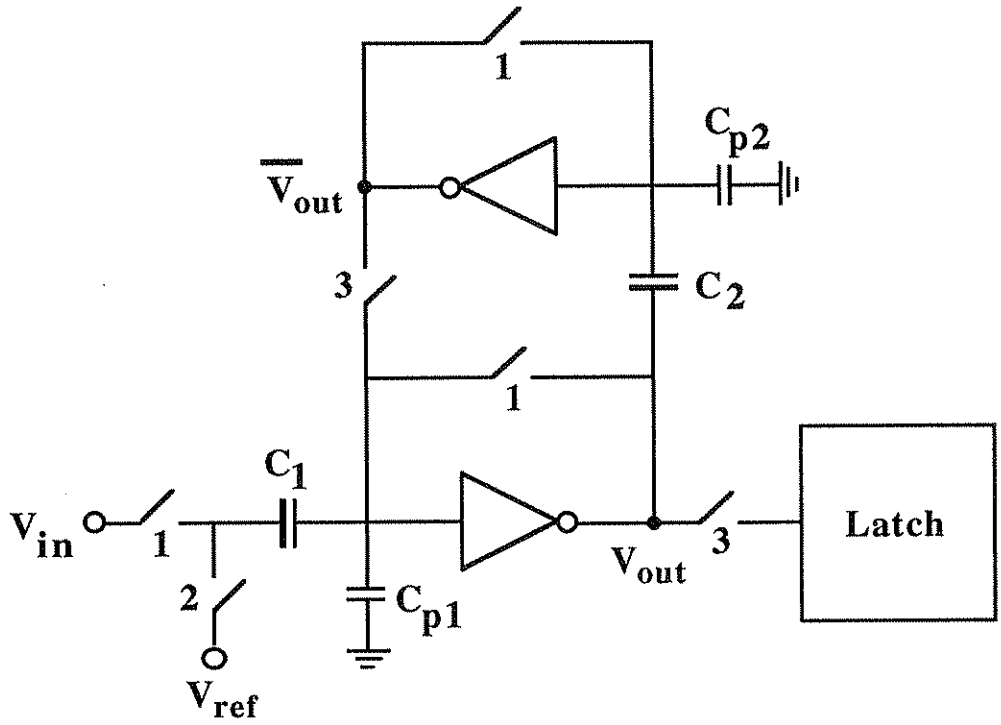


Clocking Scheme

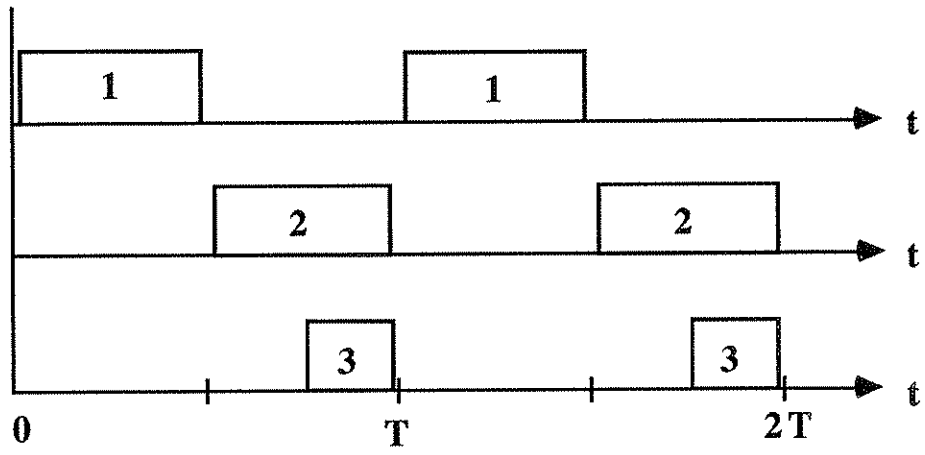


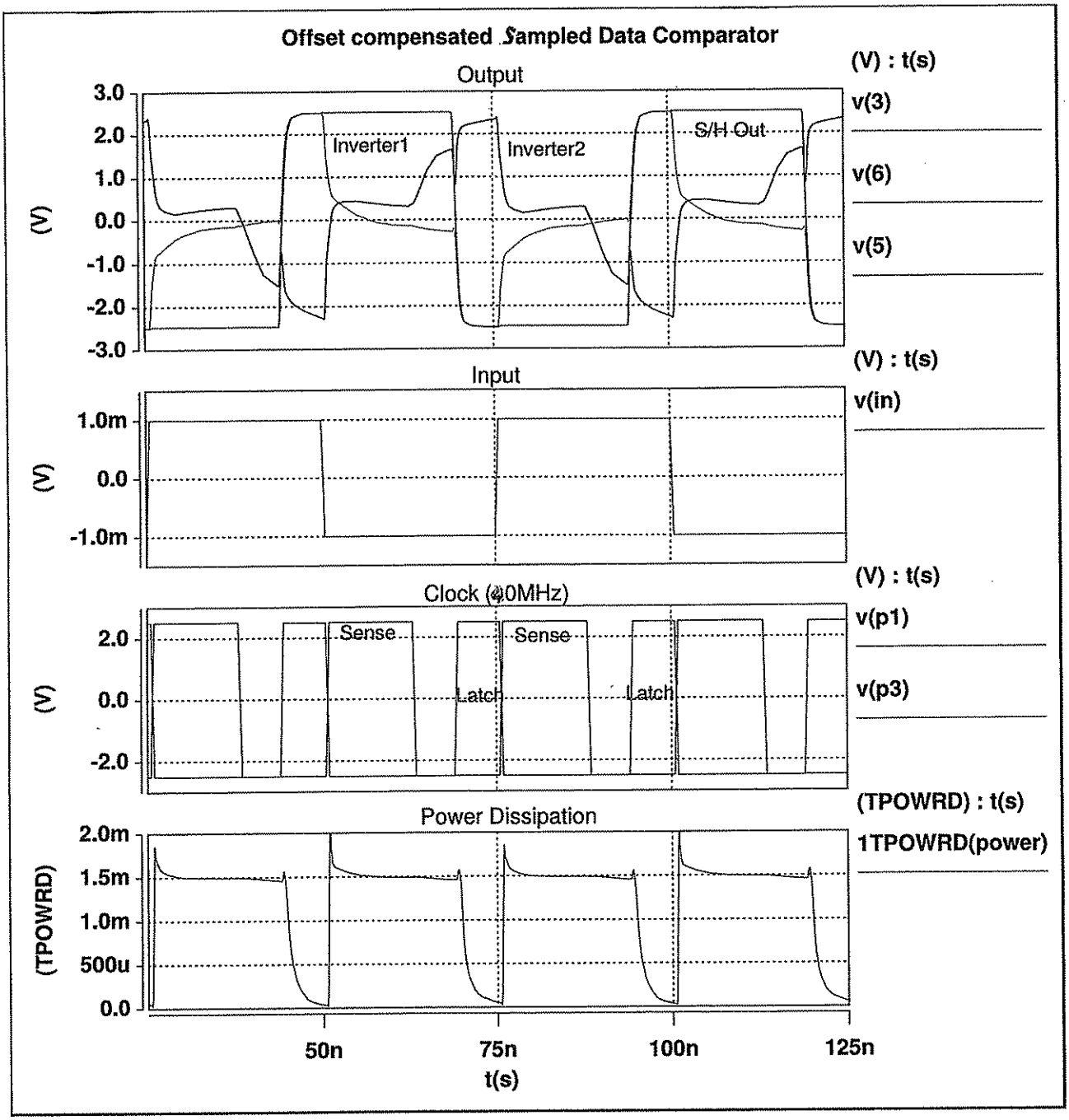

Offset compensated Sampled Data Comparator
Output
(V) : t(s)
v(5)
v(7)
Inverter3
Inverter2
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
(V)
Input
(V) : t(s)
v(in)
1.0m
0.0
-1.0m
(V)
Clock (40MHz)
(V) : t(s)
v(p1)
Sense
Sense
Latch
Latch
2.0
0.0
-2.0
(V)
Power Dissipation
(TPOWRD) : t(s)
1TPOWRD(power)
5.0m
4.0m
3.0m
2.0m
1.0m
0.0
(TPOWRD)
50n
75n
100n
125n
t(s)

Sampled-Data Comparator Version 2

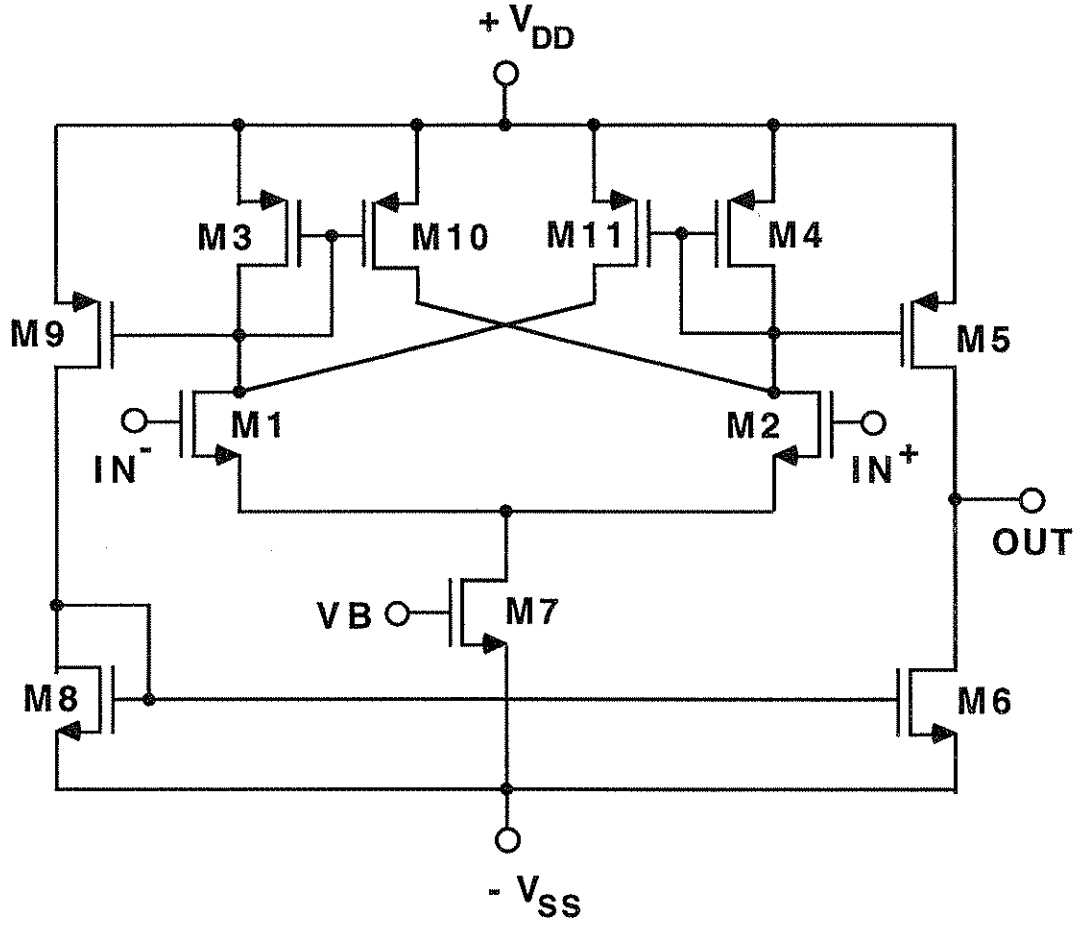


Clocking Scheme




Offset compensated Sampled Data Comparator
Output
(V) : t(s)
v(3)
v(6)
v(5)
Inverter1
Inverter2
S/H Out
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
(V)
Input
(V) : t(s)
v(in)
1.0m
0.0
-1.0m
(V)
Clock (40MHz)
(V) : t(s)
v(p1)
v(p3)
Sense
Sense
Latch
Latch
2.0
0.0
-2.0
(V)
Power Dissipation
(TPOWRD) : t(s)
1TPOWRD(power)
2.0m
1.5m
1.0m
500u
0.0
(TPOWRD)
50n
75n
100n
125n
t(s)

CMOS Comparator with Hysteresis Version 4



$$V_{Hyst} = \sqrt{\frac{2 I_7}{\mu C_{ox} \left(\frac{W}{L}\right)_1 (1+h)}} \left[\sqrt{K} - 1\right]$$

where $h = \dfrac{(W/L)_{10}}{(W/L)_3}$ $\qquad K > 1$

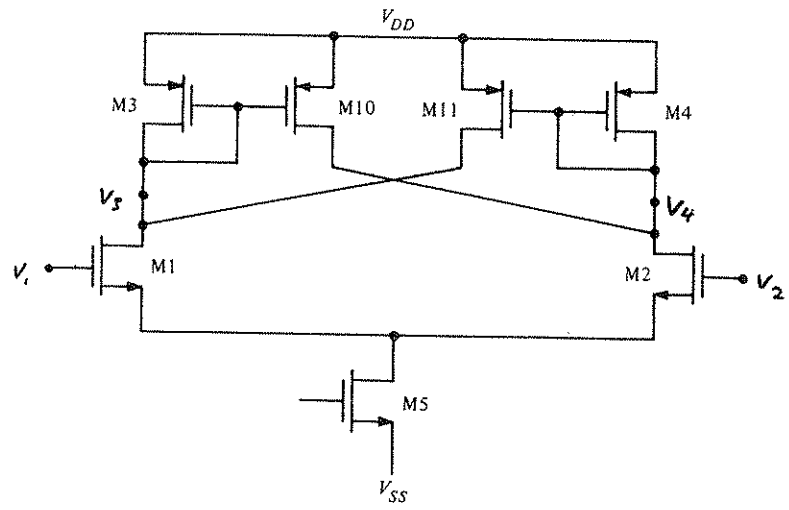
$V_{Hyst} = |V_{eff_1} - V_{eff_2}|$ @ trip point

pos. transition: $I_1 = I_3$ $\quad I_2 = I_{10} = K \cdot I_3$ $\quad I_7 = I_1 + I_2 = I_3 (1+k)$

(M4 & M11 are off)

$$\therefore V_{eff_1} = \sqrt{\frac{2 I_7}{\left(\frac{W}{L}\right)_1 \mu C_{ox} (1+h)}} \qquad V_{eff_2} = \sqrt{\frac{2 I_7 \cdot K}{\frac{W}{L} \mu C_{ox} (1+h)}}$$

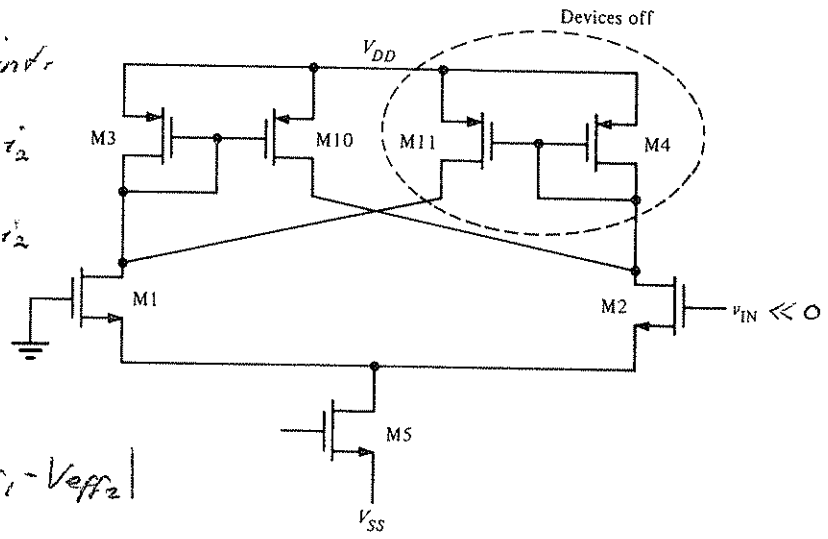
Comparator with Hysteresis



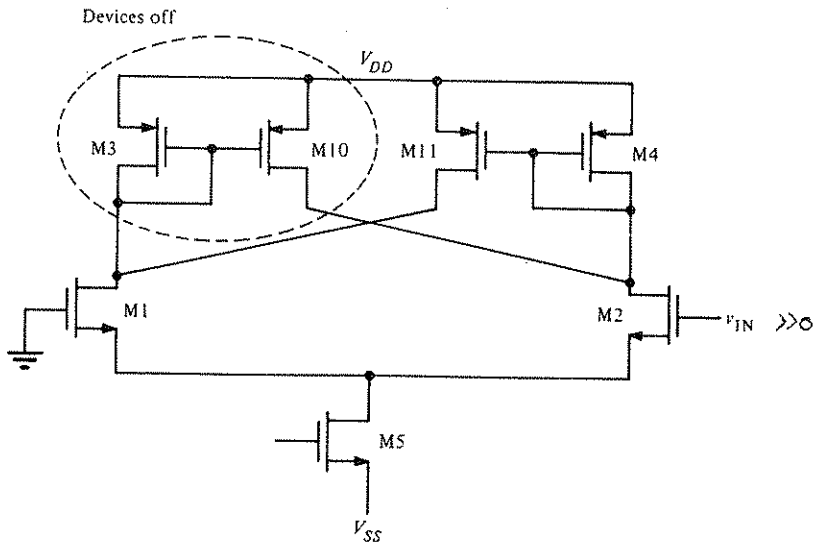
Pos. trip point:

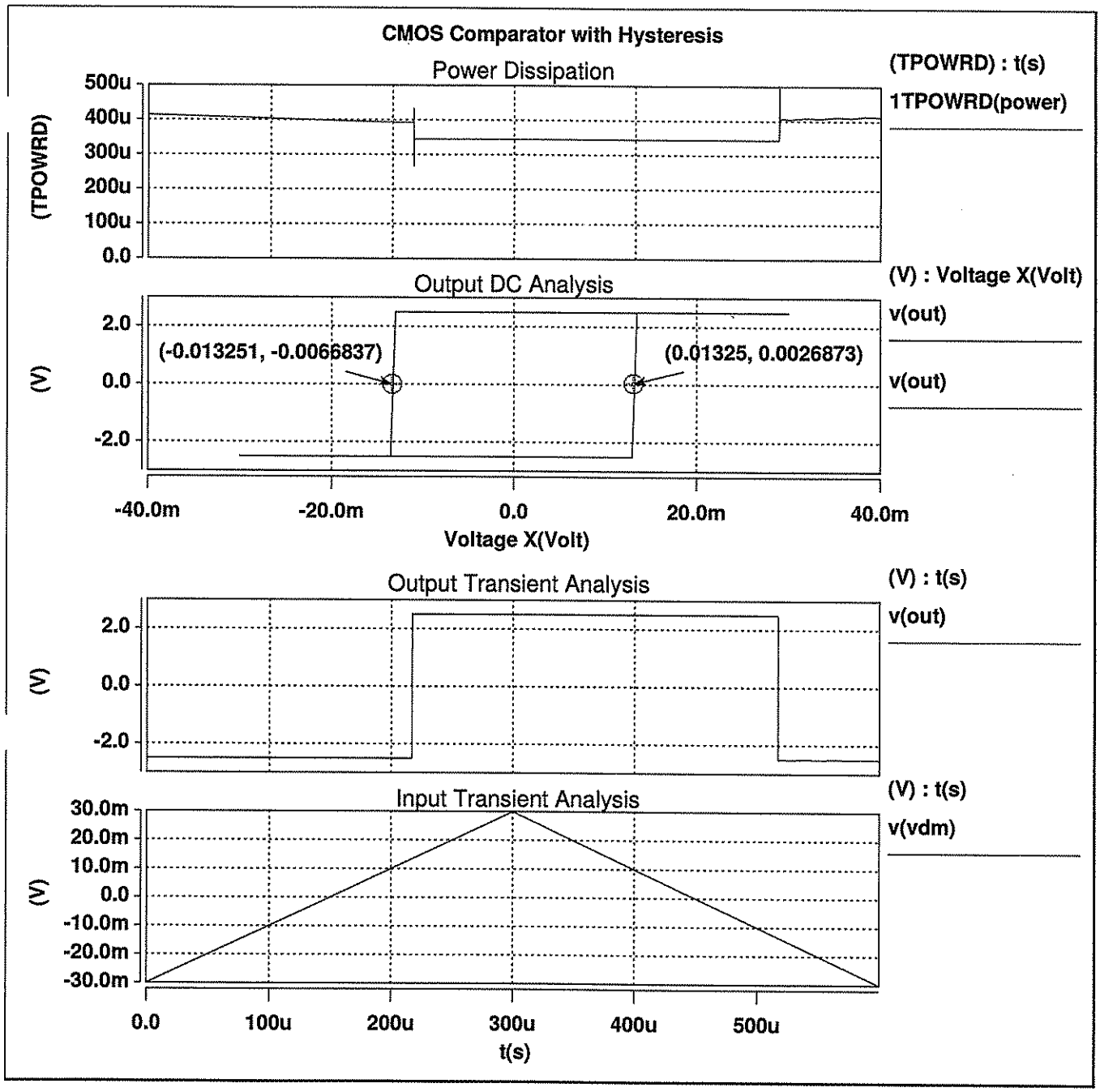
$$i_{10} = \frac{(W/L)_{10}}{(W/L)_5} i_5 = i_2$$

$$i_5 = i_1 + i_2 = i_5 + i_2$$

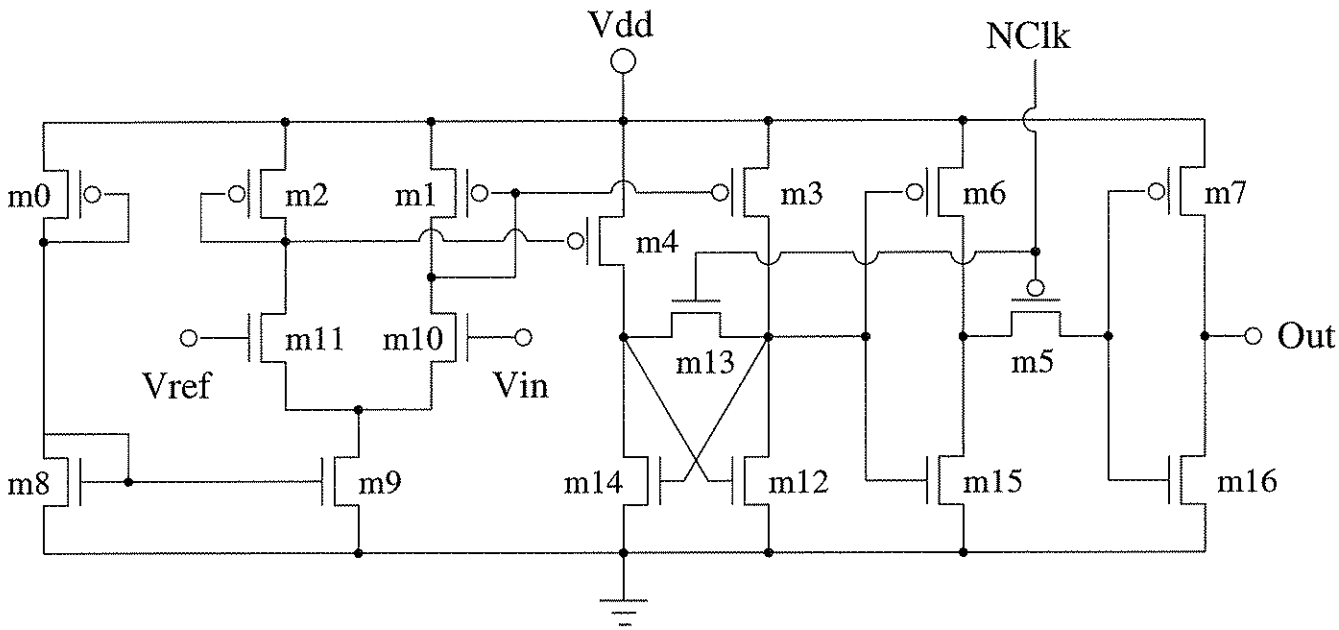


$$V_{hyst} = |V_{eff_1} - V_{eff_2}|$$

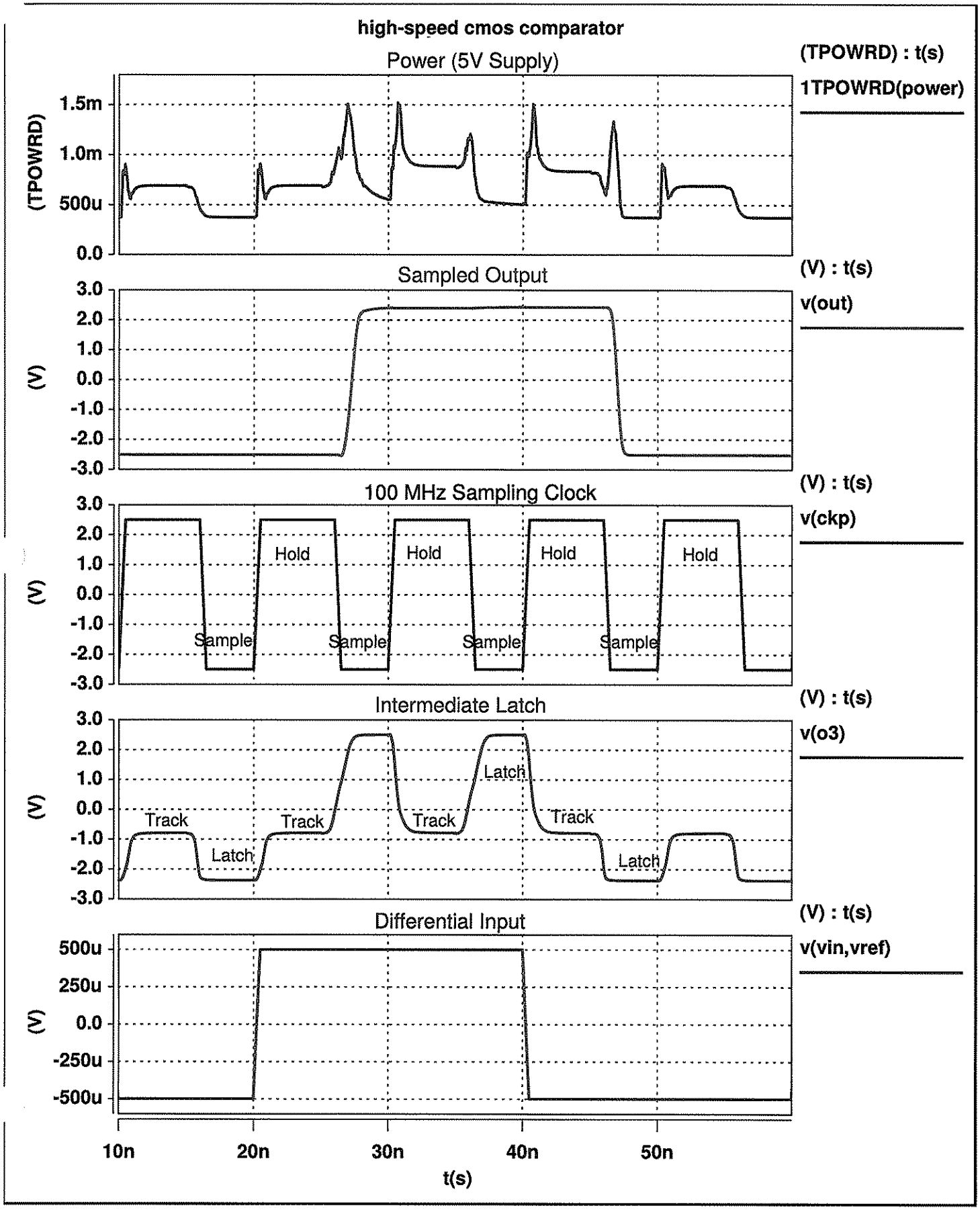



CMOS Comparator with Hysteresis
Power Dissipation
(TPOWRD) : t(s)
1TPOWRD(power)
(TPOWRD)
500u
400u
300u
200u
100u
0.0
Output DC Analysis
(V) : Voltage X(Volt)
v(out)
(-0.013251, -0.0066837)
(0.01325, 0.0026873)
v(out)
(V)
2.0
0.0
-2.0
-40.0m
-20.0m
0.0
20.0m
40.0m
Voltage X(Volt)
Output Transient Analysis
(V) : t(s)
v(out)
(V)
2.0
0.0
-2.0
Input Transient Analysis
(V) : t(s)
v(vdm)
(V)
30.0m
20.0m
10.0m
0.0
-10.0m
-20.0m
-30.0m
0.0
100u
200u
300u
400u
500u
t(s)

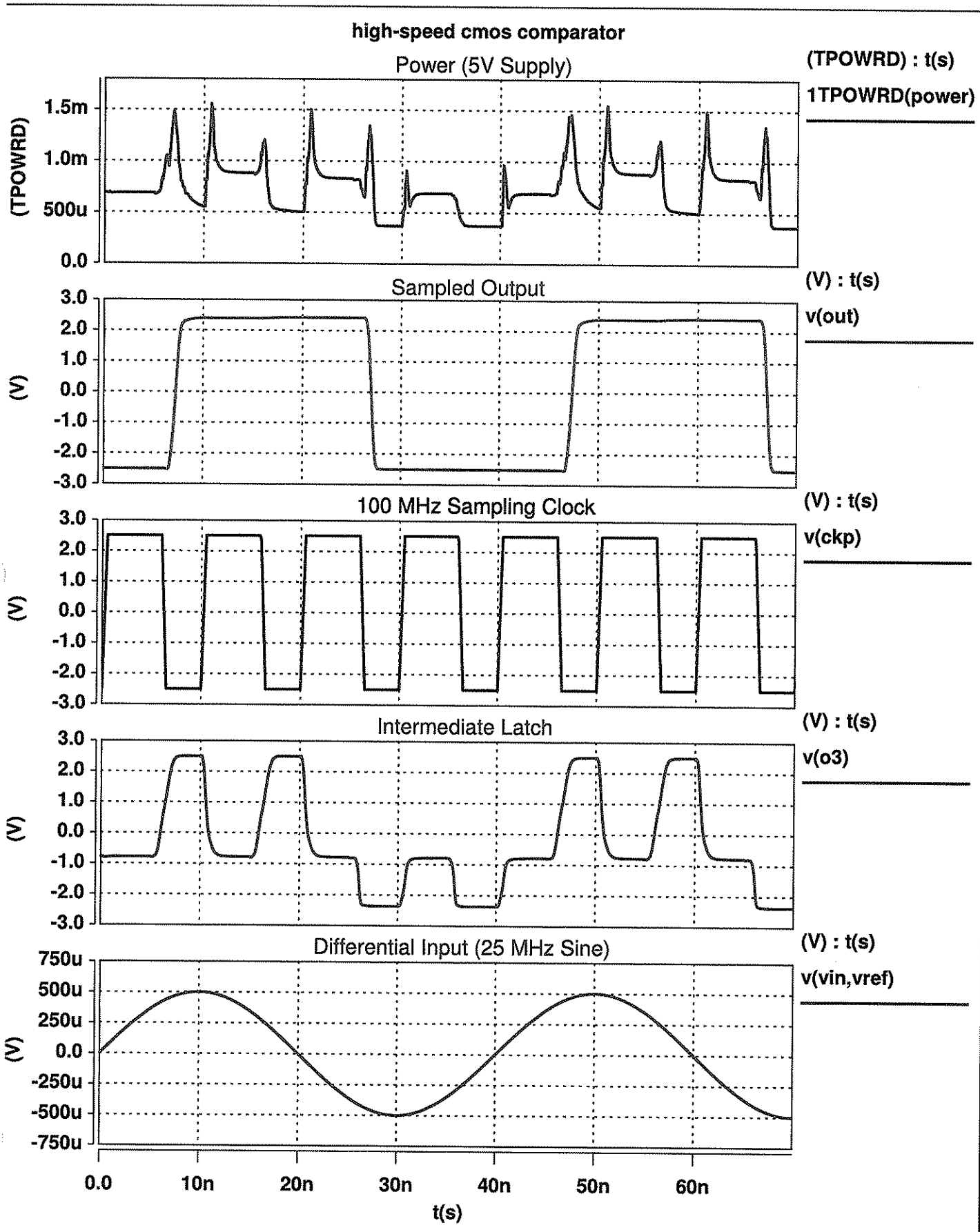
Latched CMOS Comparator



comp5_new


high-speed cmos comparator
Power (5V Supply)
(TPOWRD) : t(s)
1TPOWRD(power)
(TPOWRD)
1.5m
1.0m
500u
0.0
Sampled Output
(V) : t(s)
v(out)
(V)
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
100 MHz Sampling Clock
(V) : t(s)
v(ckp)
Hold
Sample
Intermediate Latch
(V) : t(s)
v(o3)
Track
Latch
Differential Input
(V) : t(s)
v(vin,vref)
500u
250u
0.0
-250u
-500u
10n
20n
30n
40n
50n
t(s)

comp5_new


high-speed cmos comparator
Power (5V Supply)
(TPOWRD) : t(s)
1TPOWRD(power)
(TPOWRD)
1.5m
1.0m
500u
0.0
Sampled Output
(V) : t(s)
v(out)
(V)
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
100 MHz Sampling Clock
(V) : t(s)
v(ckp)
Intermediate Latch
(V) : t(s)
v(o3)
Differential Input (25 MHz Sine)
(V) : t(s)
v(vin,vref)
750u
500u
250u
0.0
-250u
-500u
-750u
0.0
10n
20n
30n
40n
50n
60n
t(s)

comp 5_diff

high-speed cmos comparator with 2 differential input pairs