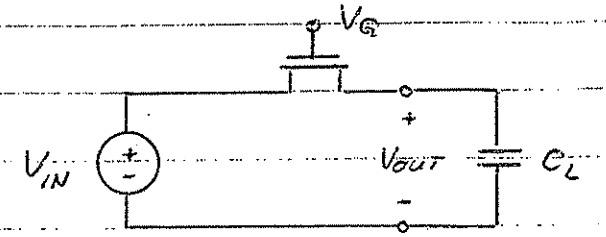
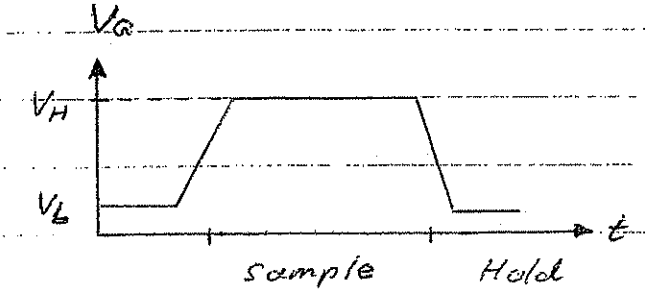
V MOS S/H Circuits

1. Basic Circuit



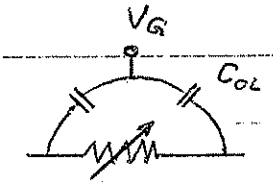


acquisition time $\tau = R_{ON} C_L$

$$R_{ON} \cong \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_t)}$$ for small V_{DS}

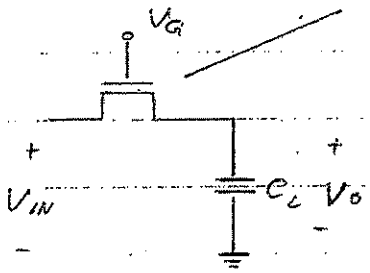
Nonideal effects

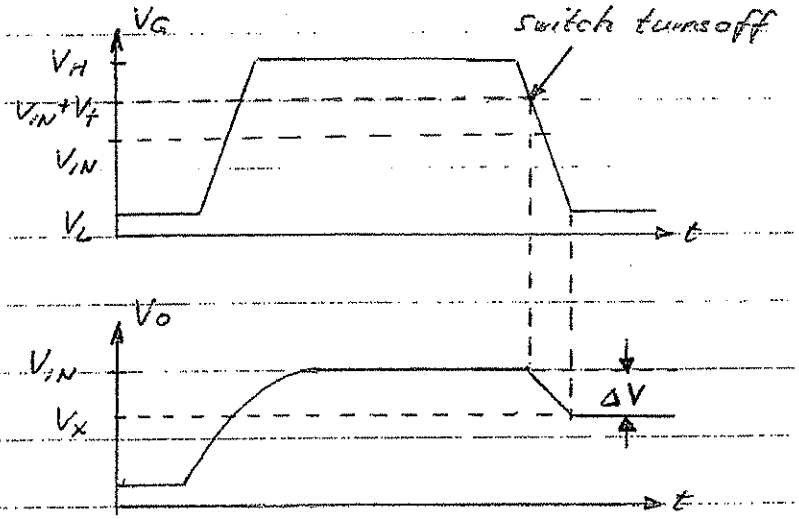
A) Slow Case



assumption:

$V_{IN} < (V_H - V_t)$





Charge balance:

$$V_{IN} C_L + (V_{IN} - [V_{IN} + V_T]) C_{OL} = (V_{IN} - \Delta V) C_L + (V_{IN} - \Delta V - V_L) C_{OL}$$

Charge at turn off — Charge in Hold state

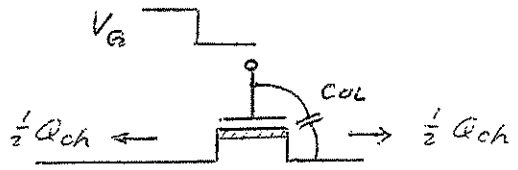
$$-V_T C_{OL} = (V_{IN} - V_L) C_{OL} - \Delta V (C_L + C_{OL})$$

$$\boxed{\Delta V = (V_{IN} + V_T - V_L) \frac{C_{OL}}{(C_L + C_{OL})}}$$

$$\boxed{V_{OUT} = V_X = V_{IN} - \Delta V = \left(V_{IN} \frac{C_L}{C_{OL}} - V_T + V_L\right) \frac{C_{OL}}{(C_L + C_{OL})}}$$

$$\boxed{\begin{array}{l} \text{Gain Error: } E_S = -\dfrac{C_{OL}}{(C_L + C_{OL})} \\ \\ \text{Offset Error: } V_{OS} = -(V_T - V_L) \dfrac{C_{OL}}{(C_L + C_{OL})} \end{array}} \quad (C_L \gg C_{OL})$$

5) Fast Case



$$Q_{ch} \cong W L C_{ox} (V_{OS} - V_T)$$
$$= W L C_{ox} (V_H - V_{IN} - V_T)$$

Charge balance:

$$(V_{IN} - V_H) C_{OL} + V_{IN} C_L = \frac{1}{2} Q_{ch} + (V_{IN} - \Delta V - V_L) C_{OL} + (V_{IN} - \Delta V) C_L$$

Charge at turn off — Charge in Hold stage

$$-(V_H - \Delta V) C_{OL} = \frac{1}{2} Q_{ch} - V_L C_{OL} - \Delta V C_L$$

$$-(V_H - V_L) C_{OL} - \frac{1}{2} Q_{ch} = -\Delta V (C_L + C_{OL})$$

$$\Delta V = (V_H - V_L)\frac{C_{OL}}{(C_L + C_{OL})} + \frac{1}{2} W L (V_H - V_{IN} - V_t)\frac{C_{ox}}{(C_L + C_{OL})}$$

$$V_{OUT} = V_{IN} - \Delta V = V_{IN}\left(1 + \frac{1}{2}\frac{WL\,C_{ox}}{C_L + C_{OL}}\right) - (V_H - V_L)\frac{C_{OL}}{C_L + C_{OL}} - (V_H - V_t)\frac{1}{2}\frac{WL\,C_{ox}}{C_L + C_{OL}}$$

Gain Error: $\varepsilon_F = \frac{1}{2}\frac{WL\,C_{ox}}{(C_L + C_{OL})}$

Offset Error: $V_{OS_F} = -(V_H - V_L)\frac{C_{OL}}{C_L + C_{OL}} - (V_H - V_t)\frac{1}{2}\frac{WL\,C_{ox}}{C_L + C_{ox}}$

Numerical Example:

$V_t = 1V$; $V_H = 2.5V$; $V_L = -2.5V$

$C_L = 250fF$; $L = 0.5\mu m$; $W = 1\mu m$

$t_{ox} = 14nm \Rightarrow C_{ox} \cong 2.5\ \frac{fF}{\mu m^2}$

Overlap Cap: $C_{OL} \cong W \cdot LD \cdot C_{ox}$

$LD = 0.05\mu m \Rightarrow \underline{C_{OL} \cong 0.13fF}$

Resulting Errors:

Slow Case:

$\varepsilon_S = -5.2 \times 10^{-4}$

$V_{OS_S} = -0.5\ mV$

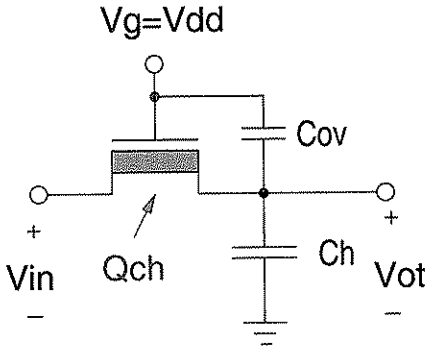
Fast Case:

$\varepsilon_F = +2.5 \times 10^{-3}$

$V_{OS_F} = -6.4\ mV$

Switched–Capacitor Sample and Hold

Track Phase (n–channel switching transistor is on)



Assumption: Vin < Vdd – Vt

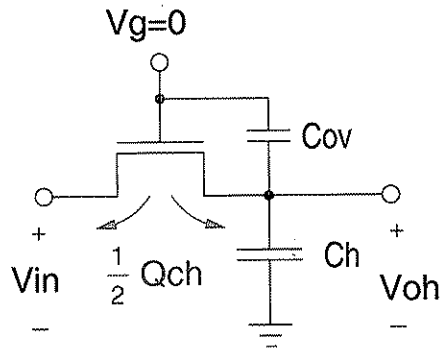
Vot = Vin

Qot = Vot Ch + (Vot–Vdd) Cov – 1/2 Qch

Qch = Cch (Vdd–Vt–Vot)

where $Cch = W\,L\,\frac{\varepsilon}{tox} = W\,L\,Cox$

Hold Phase (n–channel switching transistor is off)



Assumption: Vg switches fast

Qch = 0

Qoh = Voh (Ch+Cov)

Charge Conservation (Qot=Qoh)

$$Voh = Vin\,\frac{Ch+Cov+Cch/2}{Ch+Cov} - Vdd\,\frac{Cov+Cch/2}{Ch+Cov} + Vt\,\frac{Cch/2}{Ch+Cov}$$

Gain Error: $Eg = \frac{Cch/2}{Ch+Cov}$

Offset Error $Vos = \frac{Vt\,Cch/2 - Vdd(Cov+Cch/2)}{Ch+Cov}$

where

$V_t = V_{to} + \gamma\left[\sqrt{2\phi_F + V_{in}} - \sqrt{2\phi_F}\right]$

Charging and Discharging Hold Capacitor

Assumptions: ○ Switch is single n-channel transistor

○ $V_{in} < V_{DD} - V_t$

○ $V_{gH} = V_{DD}$, $V_{gL} = 0$

A) Charging Capacitor ($0 < V_{in} < V_{DD} - V_t$)

$$\left| \begin{array}{l} I_{D\,switch} = \beta \left[(V_{DD} - V_t)(V_{in} - V_o) - \frac{1}{2}(V_{in}^2 - V_o^2) \right] \\ r_{ON} = \dfrac{1}{\beta \left[V_{DD} - V_t - V_o \right]} \end{array} \right| \quad V_o \leq V_{in}$$

where $\left| \beta = \frac{W}{L} \mu C_{ox} \right.$

and $\left| V_t = V_{to} + \gamma \left[\sqrt{2\phi_F + V_o} - \sqrt{2\phi_F} \right] \right.$

Note: $\left| V_{o\,max} = V_{DD} - V_t = V_{in\,max} \right.$

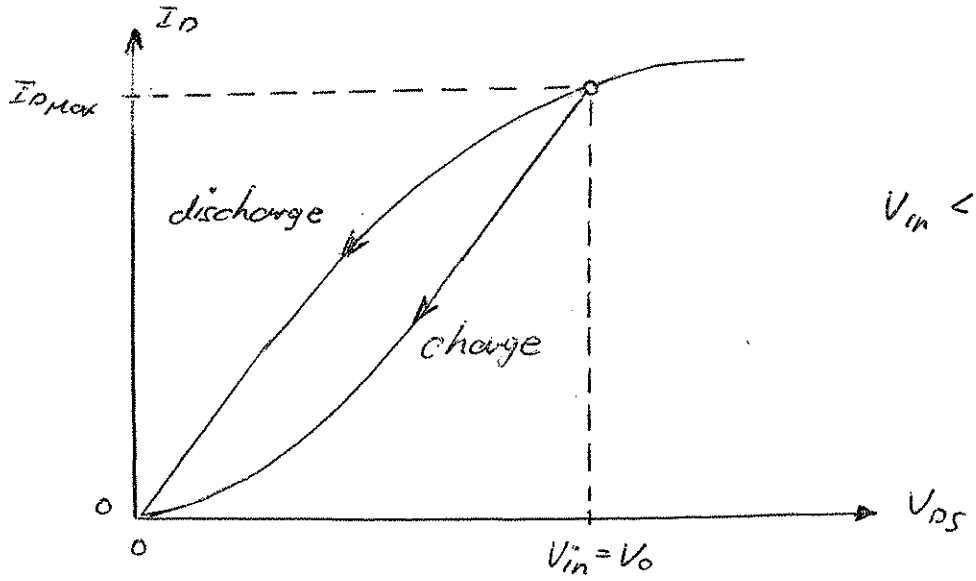
B) Discharging Capacitor ($V_{in} = 0$)

$$\left| \begin{array}{l} I_{D\,switch} = \beta \left[(V_{DD} - V_t) V_o - \frac{1}{2} V_o^2 \right] \\ r_{ON} = \dfrac{1}{\beta \left[V_{DD} - V_t - V_o \right]} \end{array} \right|$$

Time constant: $\left| \tau = r_{ON} C_h = \dfrac{C_h}{\beta \left[V_{DD} - V_t - V_o \right]} \right.$

$$\tau \propto \frac{L}{W \mu C_{ox}}$$

∴ always use minimum channel length for switching device.



$V_{in} < V_o - V_t$

$$I_{DMax} = \beta\left[(V_{DD} - V_t)V_{in} - \frac{1}{2}V_{in}^2\right]$$

$$r_{ONMin} = \frac{1}{\beta[V_{DD} - V_t]}$$

$$r_{ONMax} = \frac{1}{\beta[V_{DD} - V_t - V_{in}]}$$

Notes: V_t changes with bias, i.e. V_{in}

$\beta = \frac{W}{L}\mu C_{ox}$

Numerical Example: $V_{DD} = 5V$ $V_t = 1V$ (body effect)

$\beta = 10^{-4} A^2/V$

$V_{in} = 2V$

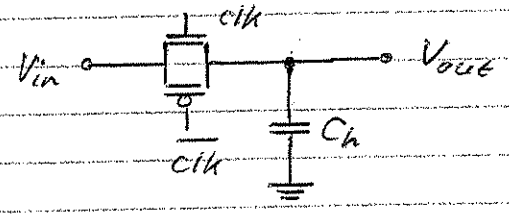
$\therefore$ $I_{DMax} = 0.6mA$

$r_{ONMin} \cong 2.5k\Omega$

$r_{ONMax} \cong 5.0k\Omega$

2. Improved Sample & Hold Stages

A) Employ composite CMOS transmission gate

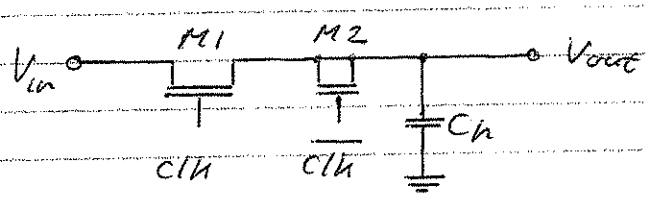


n-channel and p-channel trans. are sized equally

- Opposite channel charges of p and n-channel trans. partially cancel each other

Problem This works reasonably well for small input signals, where the 2 channel charges are closely matched.
For large signal swings, the 2 switching devices exhibit different effective voltages ($V_{as} - V_t$), resulting in poor channel charge cancellation.

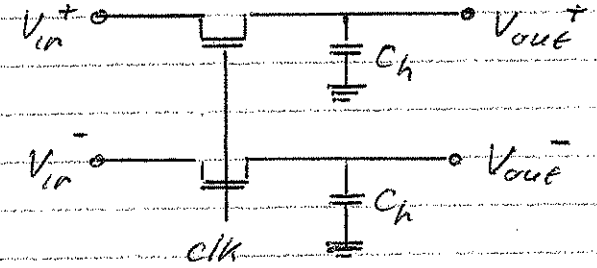
B) Add a Dummy switch



M2 is chosen at half the size of M1 ($W_2 = \frac{1}{2} W_1$) to accommodate half the channel charge of M1.

Problem The channel charge of M1 does not equally divide into a left and right side portion, thus causing an incomplete channel charge elimination.

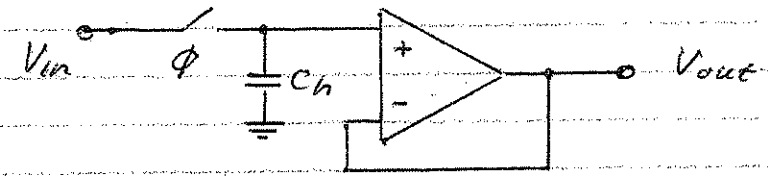
c) Differential S&H stage



This configuration eliminates common-mode errors such as offset. Gain errors, however, are not eliminated.

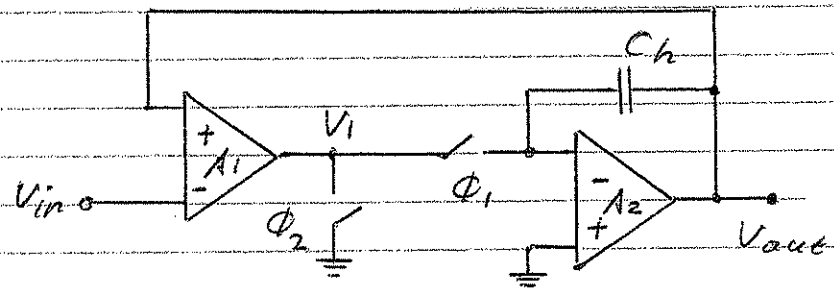
3. Active S&H circuits

A) S&H with unity-gain buffer



- Buffer adds good driving capability
- Gain error determined by passive circuit
- Buffer adds additional offset error
- Input is loaded by switch on resistor
- Buffer requires high common-mode input range

5) S/H with high Input Impedance



Φ_1 and Φ_2 are non-overlapping clocks

Φ_1 active (loop closed) → sample

$$V_{out} = V_{in}\frac{A_1 \cdot A_2}{1+A_1 \cdot A_2} \cong V_{in}$$

$$V_{1_1} = -V_{in}\frac{A_1}{1+A_1 A_2} \cong -V_{in}\frac{1}{A_2}$$

small

Φ_2 active (loop open) → hold

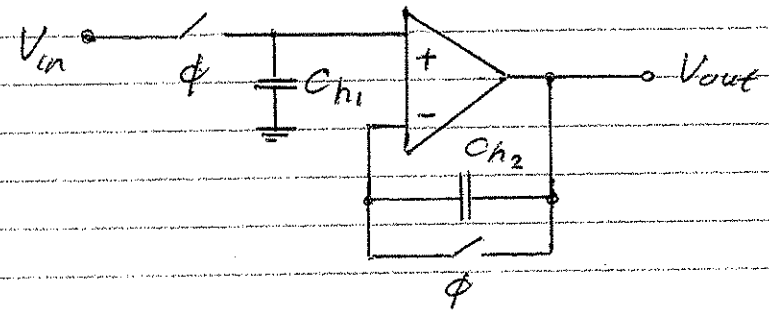
$$V_{out_2} = V_{out_1}$$

$$V_{1_2} = 0$$

Since the voltages on either side of the 2 switches are very small, charge injection errors are signal independent (offset only) and thus cause no distortion.

Problem: Speed is degraded due to the necessity to guarantee stability in the sampling mode (closed loop phase margin)

c) S/H with Clock-feedthrough Cancellation

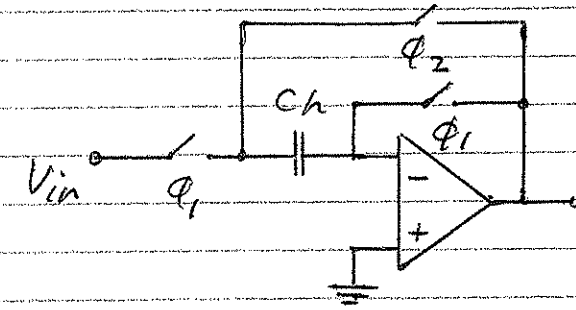


$C_{h1} = C_{h2}$

During the sampling mode (ϕ is active), the opamp acts in unity-gain configuration and the output tracks the input. In the hold mode, the input (= output) is stored across C_{h1}. Since both switches exhibit the same terminal voltages when they are turned off, the two clock-feedthrough errors are matched and suppressed by the common-mode rejection of the amplifier.

Note: The symmetry upon the switch turn-off time requires a comparatively low op-amp output impedance to match the source impedance of V_{in}.

1) Simple switched-capacitor S&H



ϕ_1 and ϕ_2 are non-overlapping clocks

sample mode (ϕ_1 is active)

Op-amp is in unity-gain mode

$$|V_{out} = 0|$$

hold mode (ϕ_2 is active)

C_h acts as the op-amp feedback and preserves the stored charge $q_1 = V_{in} C_h$

$$|V_{out} = V_{in}|$$

Note: This circuit is insensitive w.r.t. the op-amp offset voltage V_{OS}

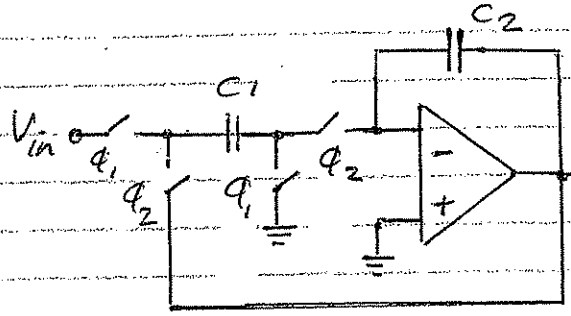
Explanation: $q_1 = (V_{in} - V_{OS}) C_h$ ϕ_1 active

$q_2 = (V_{out} - V_{OS}) C_h$ ϕ_2 active

$q_2 = q_1 \therefore |V_{out} = V_{in}|$ charge preserv.

Problem: Since the op-amp output voltage is virtually zero during the sample mode (i.e., $V_{out} = V_{os}$), a good slew rate is required to bring the output up to V_{in} during the hold mode. Obviously, the output is only valid during ϕ_2.

E) Switched-capacitor S&H and lowpass Filter



ϕ_1 and ϕ_2 are non-overlapping clocks

This circuit realizes a unity-gain 1st order lowpass filter with a cut-off frequency of

$$f_{-3dB} = \frac{1}{2\pi} f_{clk} \ln\left[1 + \frac{C_1}{C_2}\right]$$

The output voltage shows a true S&H (stairs) pattern, which reduces the op-amp slewing requirement. However, the output is not offset compensated.