Self-Healing Nanoscale Architectures on 2-D Nano-fabrics

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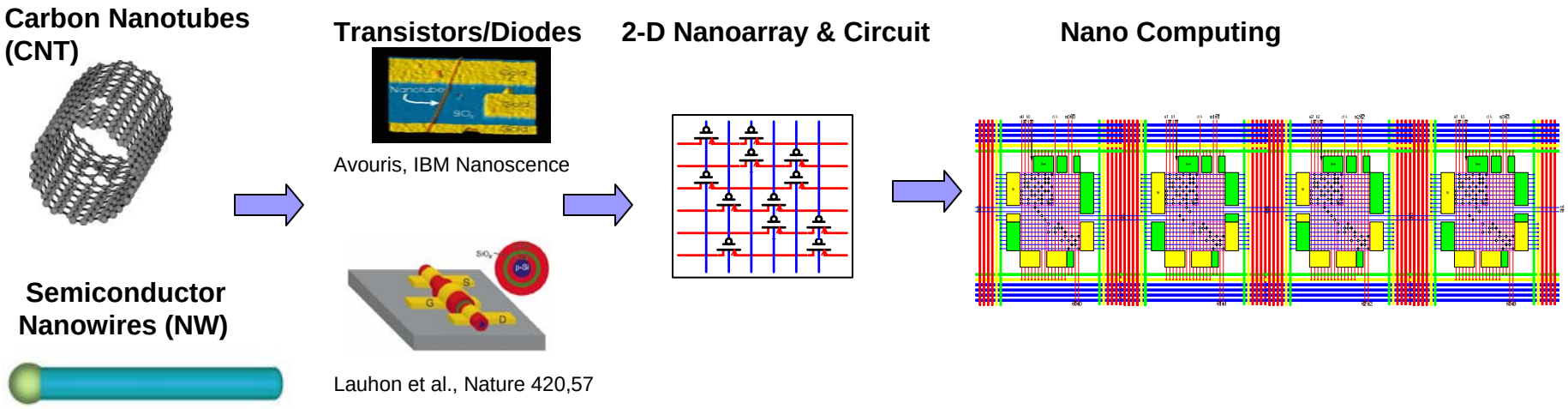
MASSNANOTECH

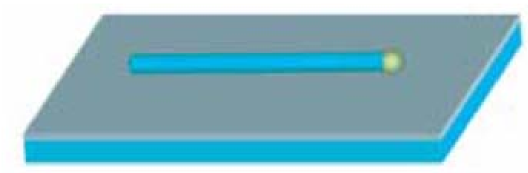
From Devices to Nano Computing



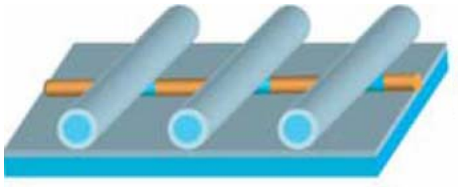
- We are trying to answer questions like
  - What are the challenges when building nanoscale circuits and architectures?
  - Can the density advantages of nanodevices be preserved at system level?
  - What would be the capabilities of such systems compared to CMOS?
  - Influence device/manufacturing research

Self Assembly of FETs and Metallic Interconnects on Nanoarray

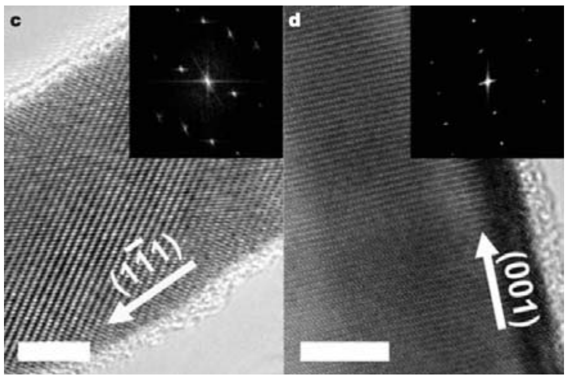
Deposit Ni (green) to Si NWs (blue)
Bake at 550°C to form NiSi (brown)



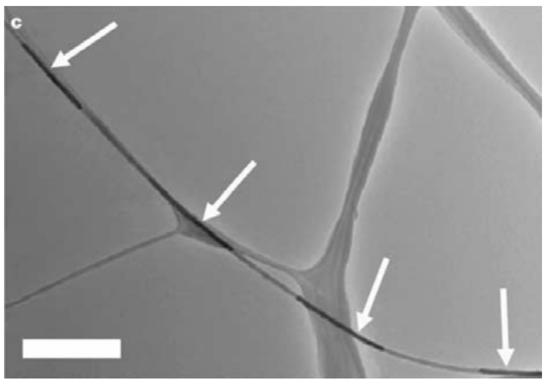
Selectively deposit Ni



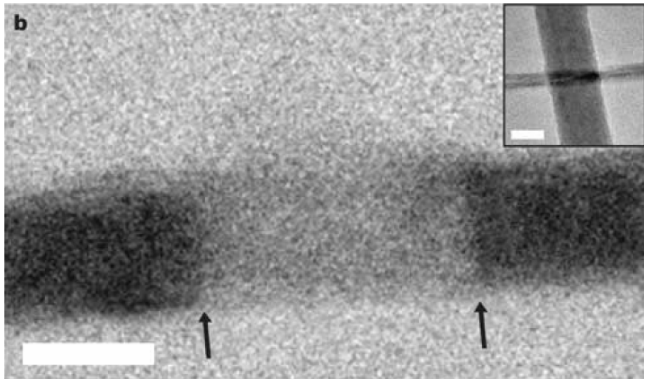
NWs as masks
Forms NiSi segments on Si NWs



Scale bar: 5nm



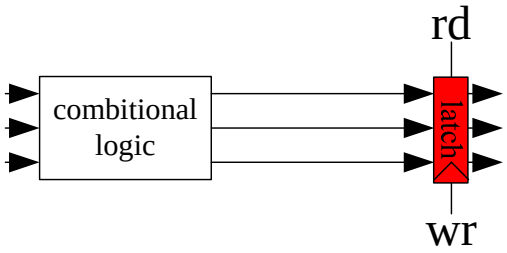
Scale bar: 1um

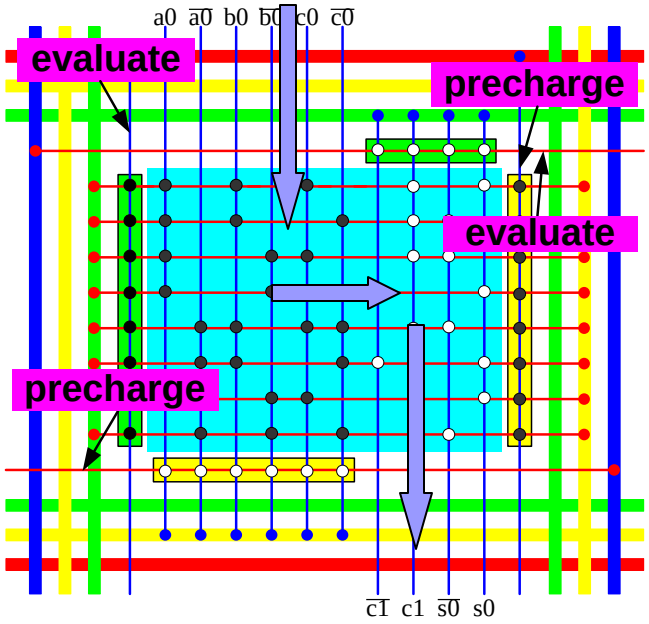


Scale bar: 10nm

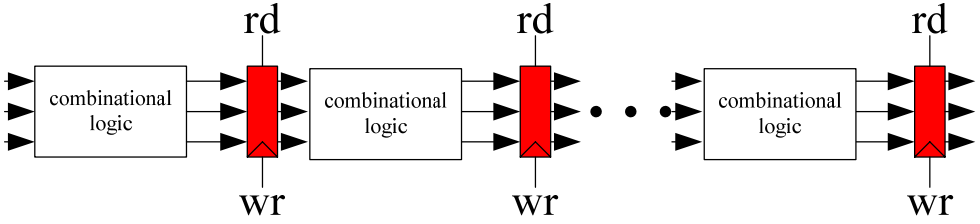
Wu et al., Nature Vol. 430, pp. 61, 2004

Dynamic NASIC Tile and Pipeline



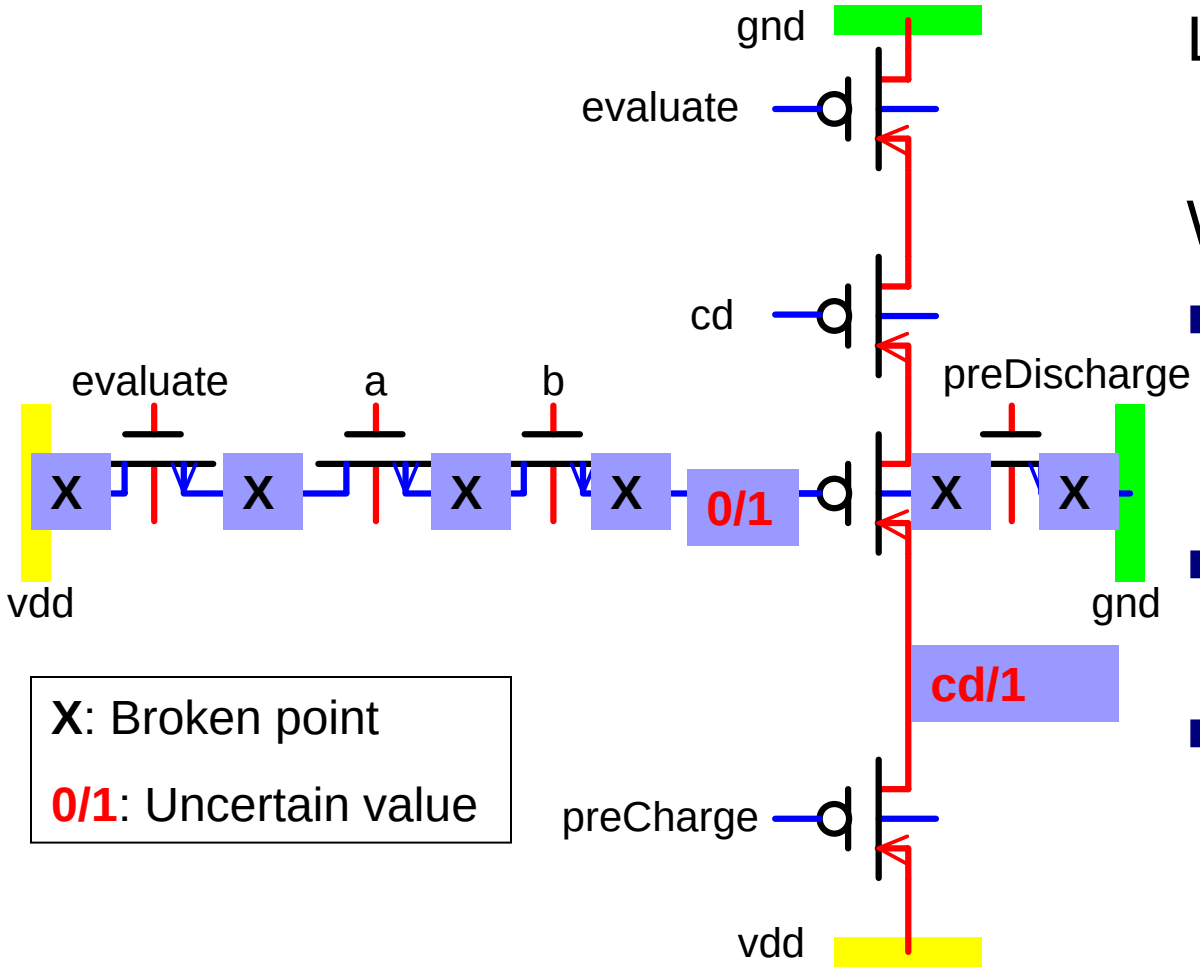


- Nano-Latch provides implicit latching on the SiNW
  - Dynamic circuit style with precharge-evaluate-hold control (see papers)
  - Solution for temporary data storage
  - Used to build pipelined structures
    - high-density stream processing



Pipelined structure

NASICs without Fault Tolerance

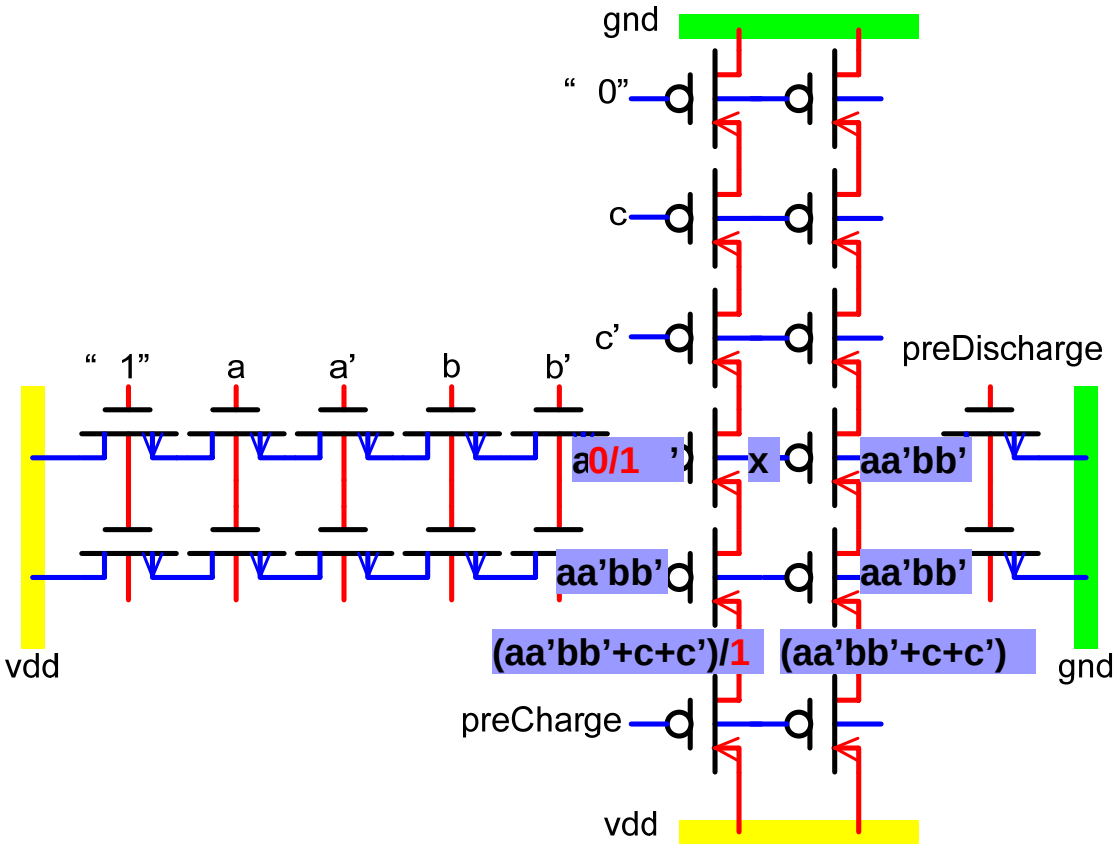


Logic: *f=ab+cd*

Without fault tolerance:

- Any fault can make the whole nanotile faulty
- We explored several approaches
- Built-in redundancy

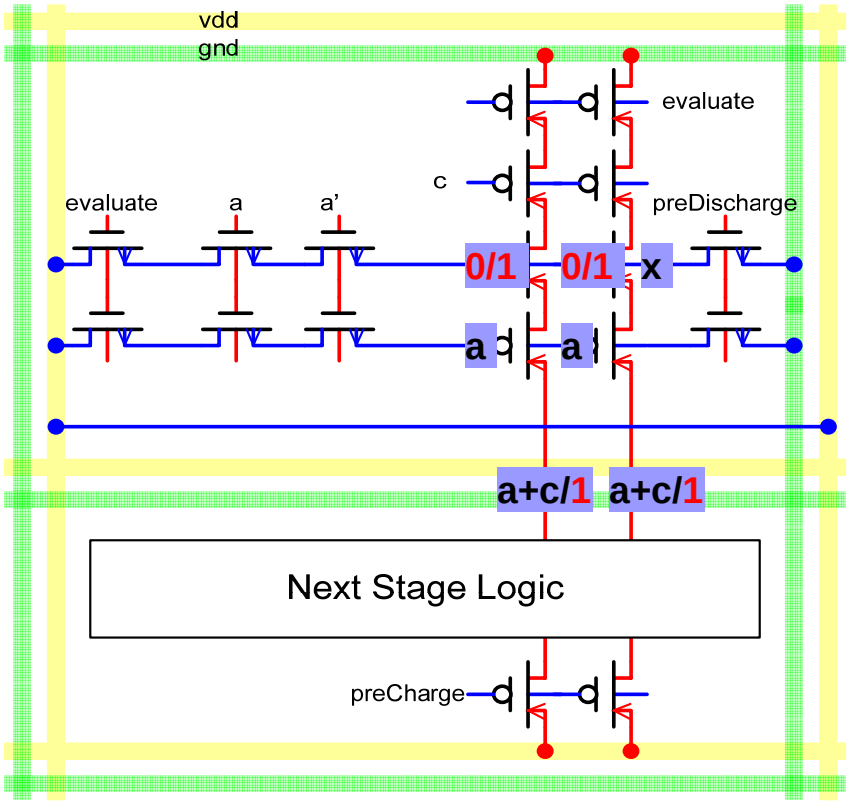
2-level Redundancy – Example



With duplicated rows:

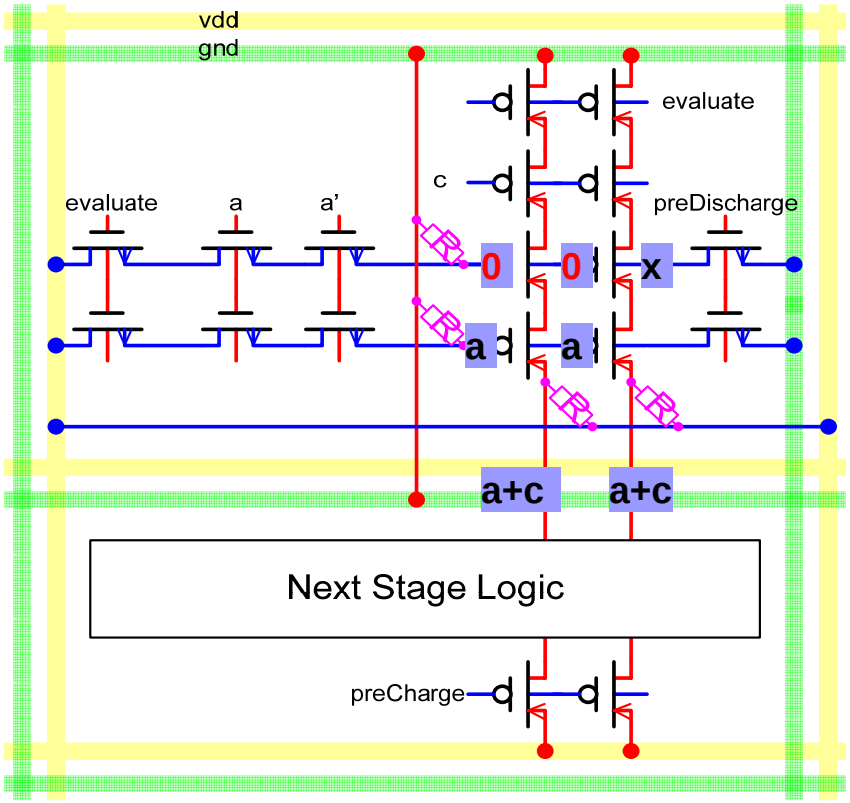
- Breaks between duplicated columns are masked by AND plane in the next stage
- Similar for breaks on the left from columns

Pull-up/down NW for Fault Tolerance



- Weak pull-up/down NWs for the case that 2-level redundancy can not handle
- Tradeoff – better fault tolerance with lower speed and power consumption

Pull-up/down NW for Fault Tolerance



- Weak pull-up/down NWs for the case that 2-level redundancy can not handle
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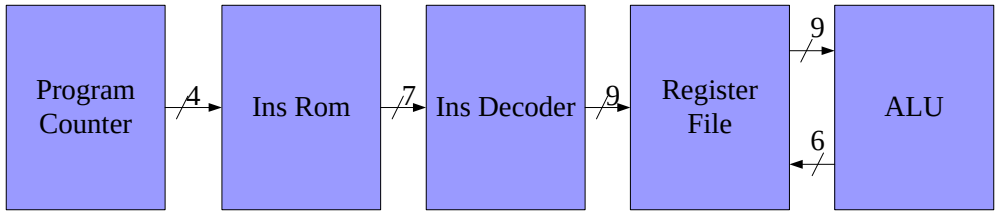
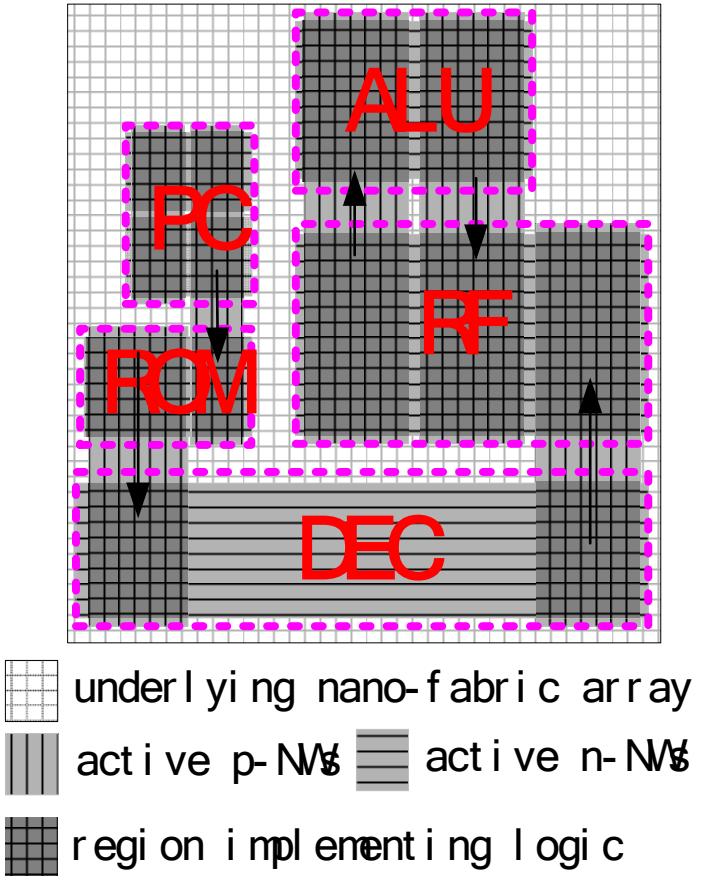
Architecture of WiSP-0

- WiSP-0 is the initial version of WiSP.
  - Supports simple ISA: *nop, movi, mov, add, mul*
  - Hazards exposed to compiler
  - Implements 5-stage pipeline on 5 NASIC nanotiles

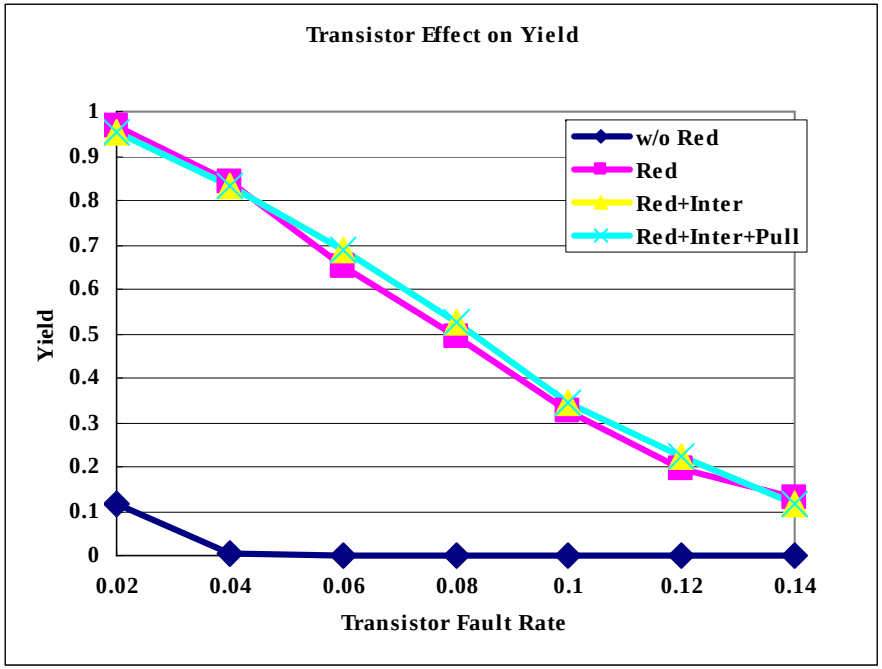


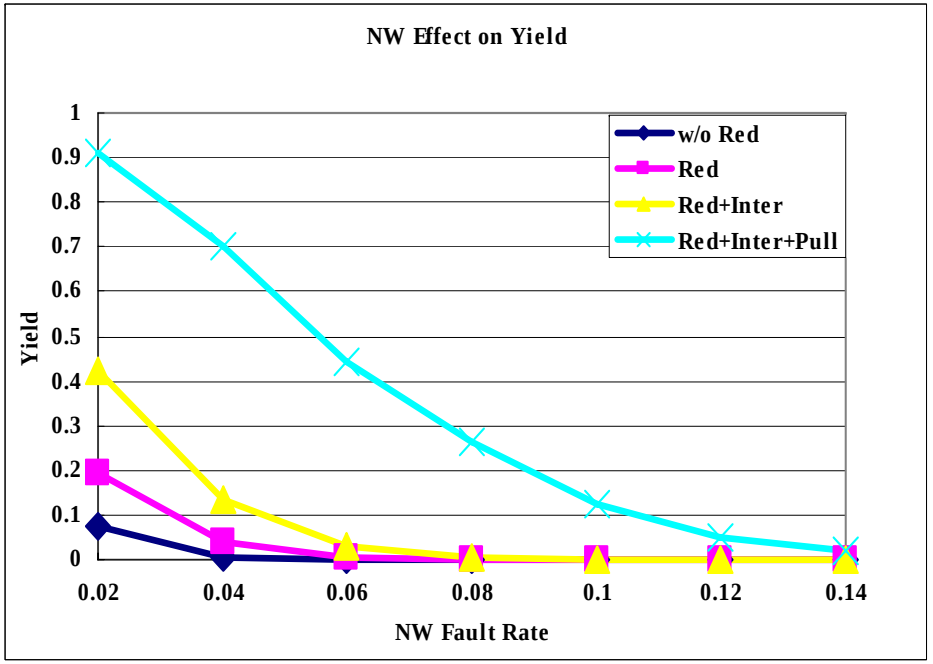
Schematic of WiSP-0



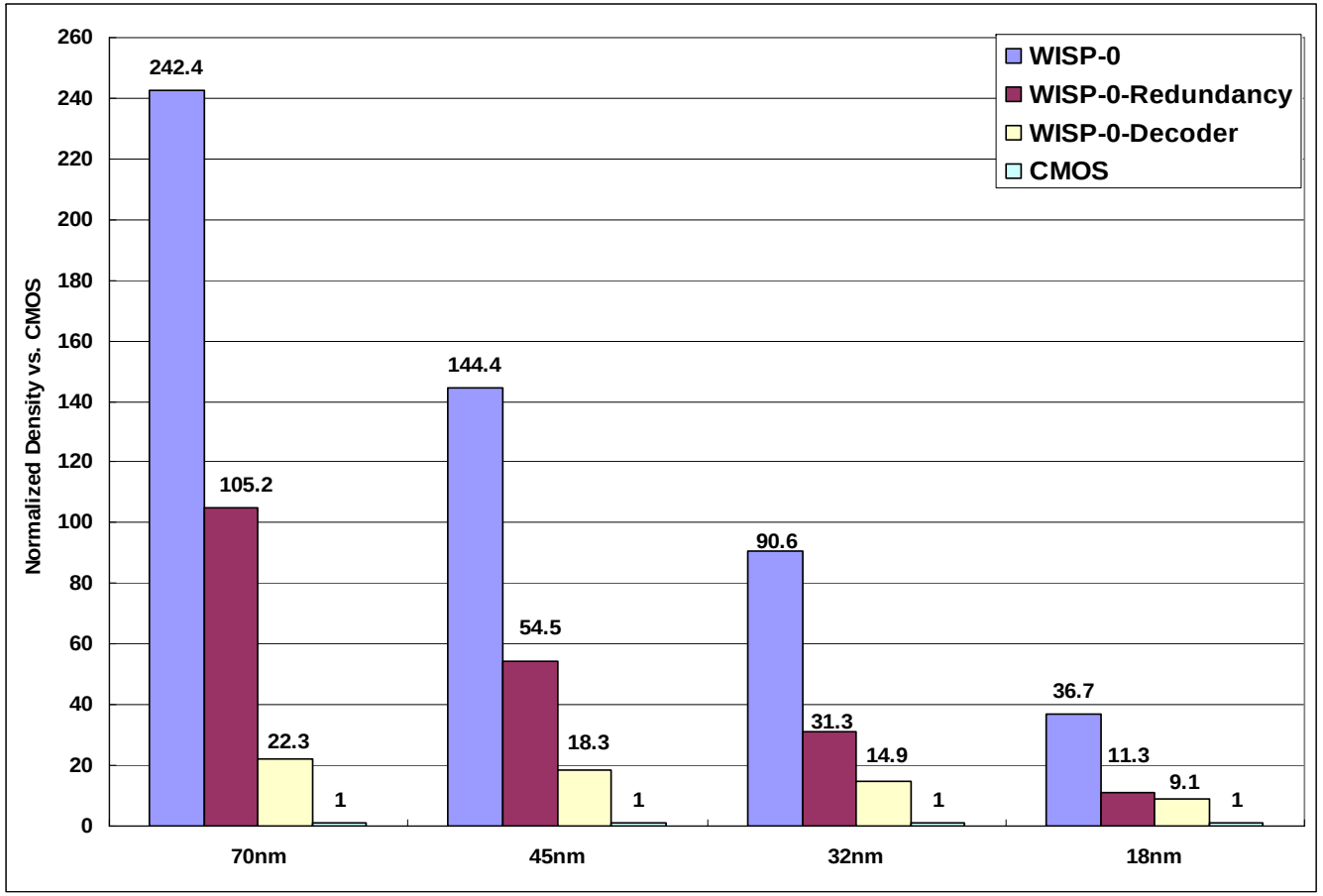
Floorplan of WiSP-0

Defect Effect on Yield





Comparison with CMOS



Conclusions

- Self-healing technique improves the yields of WISP considerably.
  - Better than 10% at 10% defect rate
- Self-healing technique eliminates the needs of decoder for reconfiguration, defect map extraction, and micro-nano alignment.
  - Significant challenge with no credible solution as yet
- Self-healing Nanoscale Architectures have great density advantage over deep sub-micron CMOS technology (11X at 18 nm).

End