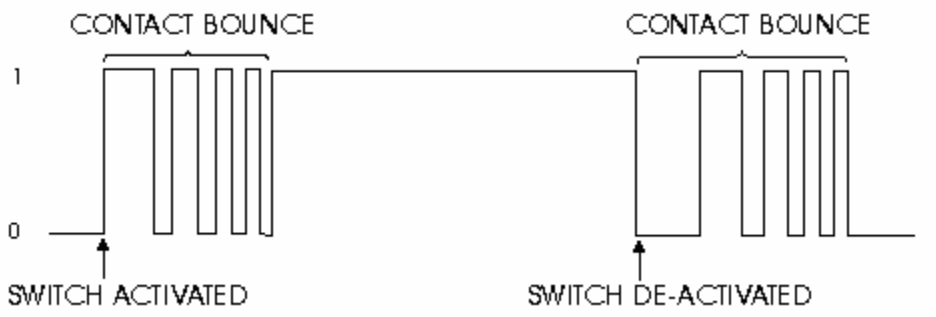
Lab 4 – Sequential Logic I ELE202 FALL2007

Objectives

- Learn about switch bounce and how to avoid it
- Build and test a binary counter, a standard sequential circuit
- Observe the utility of an MSI logic component, the 7 segment decoder

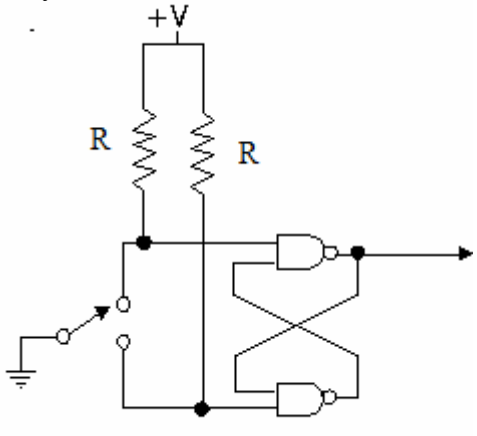
Procedure

1. Switch bounce (see page 299 of our text): Mechanical switches, including the ones on the walls of building that control lights and the ones in our lab kits for setting up signal values, make electrical connections through a set of metal contacts; the contacts conduct the current across the switch. Because they are metal, contacts have mass. And since at least one of the contacts is on a movable strip of metal, it has springiness. Further, since contacts are designed to open and close quickly, there is little resistance (low damping) to their movement. The combination of a springy mass with low damping results in "bouncy" contacts, connections that make and break several times until it settles out. In other words, when a normally open (N.O.) pair of contacts is closed, the contacts will come together and bounce off each other several times before finally coming to rest in a closed position (see the idealized figure below showing the resulting logic levels at the switch output). Note that contacts can bounce on opening as well as on closing.



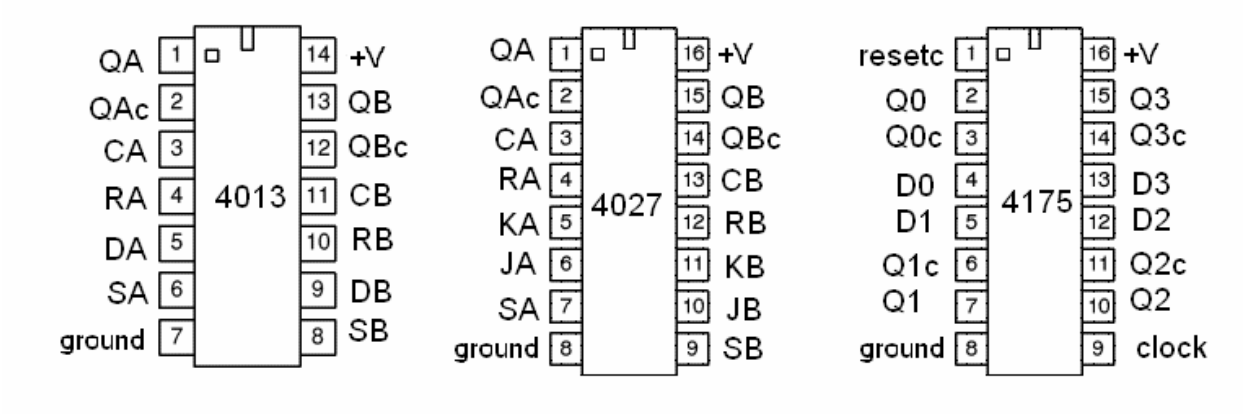
If all you want your switch to do is turn on a lamp, then contact bounce is not a problem because the bounce period is quite brief (shorter than we can see). But if you are using a switch as an input to a digital system, then you must consider contact bounce. The reason for concern is that the time it takes for contacts to stop bouncing is typically measured in milliseconds while digital circuits can respond in microseconds (or less). The result is that your system could see multiple switch actions when you only meant to have one. There are several ways to "debounce" a switch.

As shown, a common debouncer uses an SR latch made from a pair of NAND gates (4011, 2 input NANDs are available in the lab; use R = 1K Ω or larger as the pull-up resistors). The advantage of using a latch is that this circuit will respond as fast as the switch contacts can open and close; however, note that this circuit requires both open and closed contacts in the switch, an arrangement called "double throw" (the red DIP switches available in the lab bins are single pole, double throw, SPDT, so are suitable for this debouncing method). Build one debounced switch.

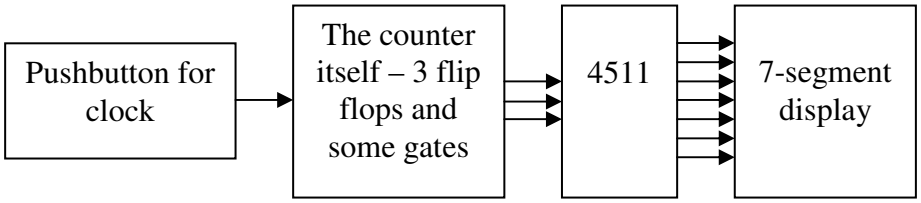


2. A typical sequential circuit that counts: Sequential circuits that cycle repeatedly through a fixed series of states are normally called counters. An example that you have already seen is the circuit within the 4520 IC – it counts in binary from 0 through 15 and then repeats (i.e. outputs 0000, 0001, 0010, 0011, 0100, 0101, … 1111, 0000, 0001, …). As described below, you are to assemble a specific counter using 3 flip flops using the debounced switch from part 1 as the clock input.

   There are several choices for flip flop ICs. Your kit contains two devices, 4013 quad-D and 4027 dual JK; we should also have 4175 quad-Ds in the bins. In the pinouts and details shown below, lower case c identifies the complement and R and S are the reset and set inputs, respectively, of each flip flop (keep these at zero on the 4013 and 4027; put resetc to 1 on the 4175). Note that on the 4175, all 4 flip flops have a common clock and reset (complemented) pin. Be sure to connect the set and reset inputs, don't leave them floating!



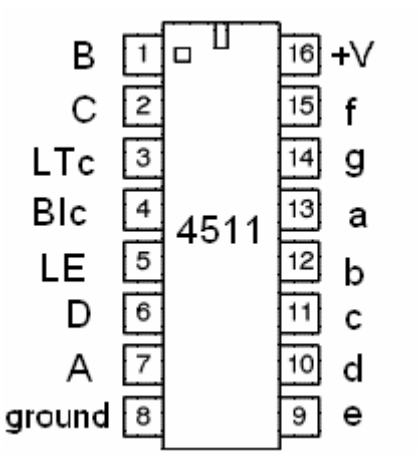
3. BCD to 7 segment decoder: To demonstrate that your circuit is displaying the correct result, you could connect LEDs to each flip flop output and watch the binary sequences. A better solution is to use combinational logic to convert those values so as to drive a 7 segment display to show the count value. A block diagram of the circuit is



   As using a display this is a common option, we have included a BCD (binary coded decimal) to 7 segment decoder IC in your lab kit, the 4511. Its pinout and truth table are shown below. The inputs are D, C, B, and A (in binary coded decimal and in that order – since we're only using 3 inputs, set D to logic 0) and the outputs correspond to segments a, b, c, d, e, f, and g of the display. The other 3 inputs provide control functions:

   - LTc – Light Test complement – this turns on all of the segments when this input is 0; hence, set this input to 1.
   - BIc – Blanking Input complement – this input allows blinking of the display (on when 1, off when 0), so set this input to 1.
   - LE – Latch Enable – this allows for freezing the display to the last value shown; set this input to 0.

REMEMBER to use 7 resistors in series with your segments (200-500 Ω is fine)!!!



inputs				*outputs*							
D	C	B	A	A	b	c	d	e	f	g	display
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	0	0	1	1	9
1	0	1	0	0	0	0	0	0	0	0	blank
1	0	1	1	0	0	0	0	0	0	0	blank
1	1	0	0	0	0	0	0	0	0	0	blank
1	1	0	1	0	0	0	0	0	0	0	blank
1	1	1	0	0	0	0	0	0	0	0	blank
1	1	1	1	0	0	0	0	0	0	0	blank

4. Assignments: For each counter below, I've listed input combinational logic for both D and JK flip flops. Note that you can mix and match; there is no need to have the same type for all 3 flip flops. Finally, assume that the numbering is Q3Q2Q1, i.e. Q3 is the most significant bit in the binary count.

   Monday: implement a downward 5 counter (i.e. 4, 3, 2, 1, 0, 4, 3, 2, 1, 0, 4, …)
   Tuesday: implement a downward 6 counter (i.e. 5, 4, 3, 2, 1, 0, 5, 4, 3, 2, 1, …)
   Wedenesday: implement an upward 5 counter (i.e. 0, 1, 2, 3, 4, 0, 1, 2, 3, 4, 0, …)
   Thursday: implement an upward 6 counter (i.e. 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, …)

When you have it working, demonstrate the counter to your instructor. Then replace the clock with a 1 or 2 kHz 555 output and display the Q2 and Q1 on a scope; again, show it to your instructor.

Monday Down 5	J3 = Q1c Q2c K3 = 1 D3 = Q1c Q2c Q3c	J2 = Q3 K2 = Q1c D2 = Q3 + Q1 Q2	J1 = Q2 + Q3 K1 = 1 D1 = Q3 + Q1cQ2
Tuesday Down 6	J3 = Q1c Q2c K3 = Q1c D3 = Q1c Q2c Q3c + Q1 Q3	J2 = Q1c Q3 K2 = Q1c D2 = Q1 Q2 + Q1c Q3	J1 = 1 K1 = 1 D1 = Q1c
Wedenesday Up 5	J3 = Q1 Q2 K3 = 1 D3 = Q1 Q2	J2 = Q1 K2 = Q1 D2 = Q1 Q2c + Q1c Q2	J1 = Q3c K1 = 1 D1 = Q1c Q3c
Thursday Up 6	J3 = Q1 Q2 K3 = Q1 D3 = Q1 Q2 + Q1c Q3	J2 = Q1 Q3c K2 = Q1 D2 = Q1 Q2c Q3c + Q1c Q2	J1 = 1 K1 = 1 D1 = Q1c

A final note: keep the 4511 and the 7 segment display wired for lab 6.

ELE202 Summary Report Form
Lab 4 – Sequential Logic I

Lab day (circle one): Mon Tue Wed Thur

NAME

Demonstrations:

Portion	Observed by	Date
Proper count with pushbutton clock		
Proper count (Q2Q1) on scope		

Score: /10 pts.