ELE202 Fall 2007 LAB5: Software Tools

We are meeting this week at Kelley 117.

ELE Account: The machines in the Department's Computer Center (Kelley 117) are running on Gentoo Linux with KDE (K Desktop Environment). *You must get an ELE account* to use these machines, which can be obtained from ELE System Manager in Kelley 117. A storage area is granted for each ELE account designated as the folder /u/ugrads/*your_name* where *your_name* is your login name. Each account is allocated 50 megabytes of disk space on our main ELE server. You will also automatically get an ELE email account: yourname@ele.uri.edu

Quartus II: The software tool for this week's lab is Quartus II from Altera. This is the software tool we are using in the ELE306; the next level logic design course. The software is designed to work in conjunction with the FPGA (field programmable gate array) for rapid prototyping of logic design hardware. In this case, we will only use its "schematic capture" and "circuit simulation" features.

Exercise

Step 1: Create and Configure the Project

- The main program used for the labs is electronic design automation (EDA) tool by *Altera* called *Quartus II*. The current version is 7.0. To start the software, click the "Start (K Menu icon)-> Run Command…". Type in "**quartus7**" in the window and hit return. Be sure to use all lowercase letters since Linux is case sensitive. The program may take a moment to start. NOTE: the quartus II program runs from server; meaning that the program has to be loaded to your local machine first and thus the loading time varies.
- To start a new project, click "*File->New Project Wizard"*. Once the wizard window appears, click the **Next** button past the introduction. The three fields presented on next page specify what directory, project name, and top-level entity are used. For simplicity, all the three fields should specify "lab5_yourname". In the first field (topmost), add "*lab5_yourname*" so it shows /u/ugrads/yourname/lab5_yourname (where "yourname" is your account name). Type in "*lab5_yourname*" to the second field and the third field will be filled automatically.
- **Remember to click on "Next"** not Finish yet!!! Click Yes to create this new directory.
- On page two, click next since there is no file from other projects that we want to import.
- On page 3, select the followings:
    - Family: "FLEX10K"
    - Target device: Specific device selected in 'Available devices' list
    - Available devices: select EPF10K70RC240-4 (last one on the list)
    - Filters: choose 'any' for all three fields. If you do see EPF10K70R240-4 in the available devices list, ignore this field.
- Skip page 4 as we do not use additional EDA tools.

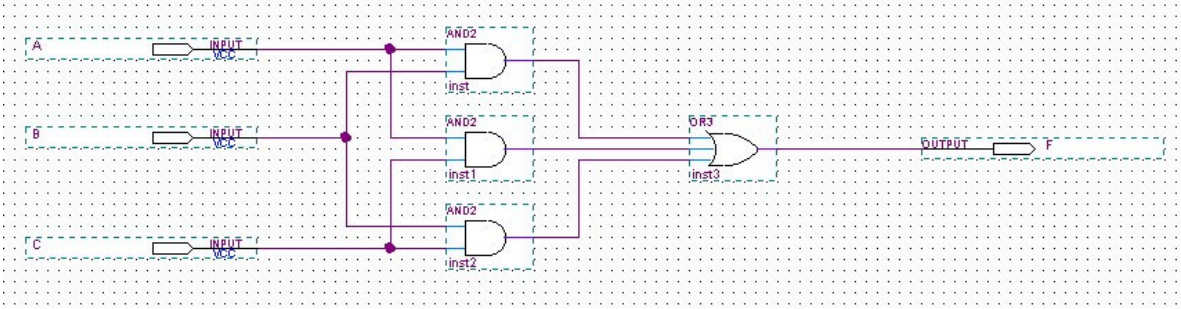
- Page 5 is a summary page of your project settings. Click Finish to complete the process of creating the project.

Step 2: Drawing the circuit

- "File->New" and select "Block Diagram/Schematic File" under the "Device Design Files" tab.
- The objective of this exercise is to create a simple logic circuit using the schematic editor. To accomplish this task, we implement the following logic functions.

$$F = AB + AC + BC$$

- Click on the "AND gate" symbol (third from top) on the vertical tool bar on the left or simply double click anywhere in the schematic window. A window titled "Symbol" appears. Double click on the library directory to see the entire directory tree. For now you may go directly to "primitives/logic" directory where you will find all the primitive logic gates you'll need. Alternatively, you may type the name in the "Name" field if you know the name of the primitive you want.
- Pick "and2" (2-input AND gate) or type "and2" in the Name field and click OK to insert the AND gate.
- Follow the same process from the previous step except to insert two more 2-input AND gates and one three-input OR (or3) gate. Finally, insert three inputs (symbol "input" under primitives/pin) and one "output" on the schematic. Double click on the input or output symbol will bring out the property window. In the "Pin name(s)" field type in the appropriate names: A, B, C and F, respectively.
- Now the wiring of the devices will be described. Left click and drag from one point to another point will create a connection (or a wire). Repeat the process until you complete the function along with connected inputs and output. The circuit should appear to be something similar to the following diagram. Save the file, print out the circuit schematic to be included in the lab report and then proceed.



Step 3: Create netlist and select simulation mode

- Click *Processing->Start Compilation* to process your schematic design. If you made a mistake in creating the circuit, the software will give you a warning at this time. If everything is fine, your schematic is now being translated into optimized Boolean equations and a proper netlist is generated (a list of logic gates and how they are connected to represent your design).

- Click *Assignment->Settings* to bring out the Settings window. Click on "Simulator Settings" to view the simulator default. Change the Simulation mode to "Functional". This will allow your design be simulated by the software even though you did not do anything yet to associate it with the real hardware.

Step 4: Functional Simulation

Since there are three binary inputs, the simulation is pretty basic with an end result of 8 possible sets of input states.

- Click *File->New* and choose the *Other Files* tab. Select *Vector Waveform File* and click *OK*.
- Now that a file is created, the nodes that are being analyzed need to be inserted. To do this click *Edit->Insert->Insert Node or Bus*.
- Click the *Node Finder* button to assist in selecting the available nodes. Verify that the field Named contains "*" and Filter contains *Pins: all*. Click *List* to have the available nodes listed. Once filtered, all available nodes or Pins (A, B, C and F) are listed in the *Nodes Found* field. To transfer a node to the waveform editor, highlight the name and click the ">" button. Since we want to test all nodes in this lab, click the ">>" button and then *OK*. As many nodes were selected, the *Name* field of the *Insert Bus or Node* window will contain "**Multiple Items**" to represent the many names. Click *OK* to proceed to add the nodes to the waveform editor file.
- *Edit->End Time* and select a time of 1000ns (or 1μs). This will display the entire length of the 8 possible states of input.
- Highlight a row by clicking on the name. Then right click *Value->Clock* or the fifth button up from bottom on the vertical toolbar on the left side (the button with a waveform and stop watch symbol). This button is used for assigning a clock signal to the input. As in Lab 2, we will put clock signals with different frequencies into A, B, and C.
- For the first signal A, use 400ns as the Period (do not change any other settings). Following the same procedure for the other two inputs, B's period is 200ns and C's period is 100ns. You have now completed the "command" file to the simulator. Save it before proceed to the next step.
- Click *Processing->Generate Functional Simulation Netlist*. This will produce the appropriate netlist (a text file that describe the logic gates and connections between the logic gates of your circuit) for the functional simulation below.
- Simulation is done by clicking *Processing->Start Simulation* from the drop-down menus. A different file will be generated for the simulation result (it looks very much like your input file but this one is not editable!)
- Verify that the desired output is generated. To do this, use arrow keys, <- and ->, to navigate through the waveforms. The magnifying glass symbol is for the zoom features. The time will be shown on top of the cursor (a light blue vertical line). You may go to print menu at this point to print out the simulation waveforms.

Lab 5 Assignment and Report:

- Recreate the circuit you've made in Lab 2 using the above procedure. Process and simulate the circuit. Verify the results making sure that your circuit is working properly.
- Your report should include: print outs of your schematic and simulation waveforms.