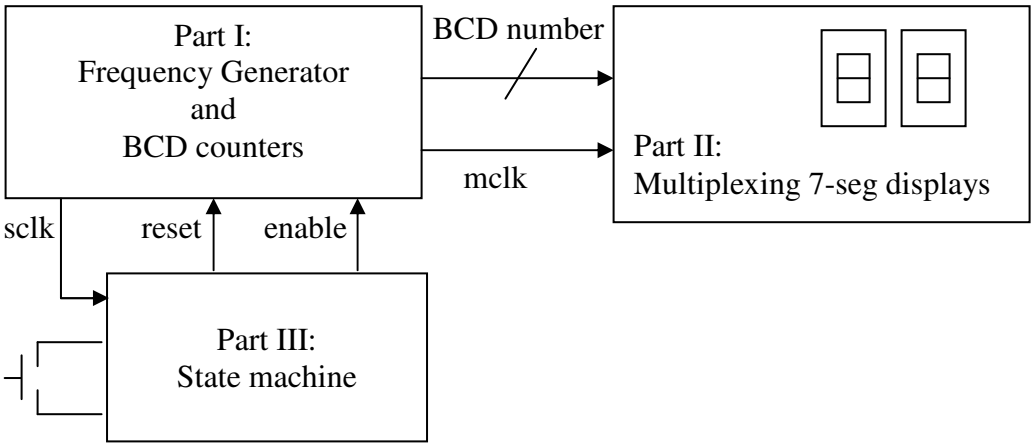
Lab 8 – Application I: BCD Counters ELE202 FALL2007

Objectives
- Learn how to use existing register-level or MSI modules and components.
- Build, and test cascaded BCD counters for multi-digit counting.

Overview
This is the first of the three labs where the end product is a stopwatch. In this one-week lab, you will begin by building the frequency generator and the BCD counting parts of the stopwatch. The block diagram (a high-level abstract view of the logic circuits in conceptual blocks) of the stopwatch is shown below: I scheduled one week for this lab and two weeks each for the next two labs. This timeline is meant as project progress milestones. You should try to be ahead or on the schedule. You should also proceed to the next lab once you finish the previous one.



The stopwatch will have two digits for counting from 0.0 to 9.9 seconds. In Part I, we will first use 555 to generate a 2560Hz clock, and then use the frequency divider, 4520, to reduce that down to 10Hz. We will use both counters in 4520 to produce clock signals of 1280Hz, 640Hz, 320Hz, 160Hz, 80Hz, 40Hz, 20Hz and finally 10Hz. The 10Hz clock signal will obviously be use in the BCD counting with two 4510's. The other higher frequency clock signals will be used as the mclk to part II and sclk to part III. These will be discussed in the next two labs.

Part II consists of 4511, the BCD to 7-segment display decoder as in lab 4. In this case, we will use only one 4511 to decode for two displays. The two displays will be multiplexed; only one display is turned on at a time, while the input to 4511 will be appropriately chosen also on the fly. The multiplexing frequency is determined by mclk. Combining Part I and Part II, we have a straightforward timer that endlessly counting from 0.0 to 9.9 and then repeat the entire sequence over.

Part III is the heart of the stopwatch. It handles the input signal from the push button (momentary switch) and generates signals: reset and enable that control the BCD counters.

NOTE: The datasheets of all the IC's used in the lab are available at the lab. They are also mostly available on the Internet as these are mostly public domain information.

Procedure

It is suggested that you should read the following steps completely first. Draw a schematic that include the entire circuit (for this lab) from the bit and pieces of information from each step. This will give you the overall view of this lab and can help you not only in understanding what you need to accomplish but also how to budget your proto-board utilizations.

Step 1:

First determine the values of Ra, Rb and C so that 555 will generate a 2560Hz clock signal. Use the formula found in lab 1. Remember that only a few particular values for resistors and capacitors are available. If you cannot generate 2560Hz exactly, you should try to limit the error to ±10%.

Step 2:

Use both counters of 4520 to generate a 10Hz clock signal from the 2560Hz signal above.

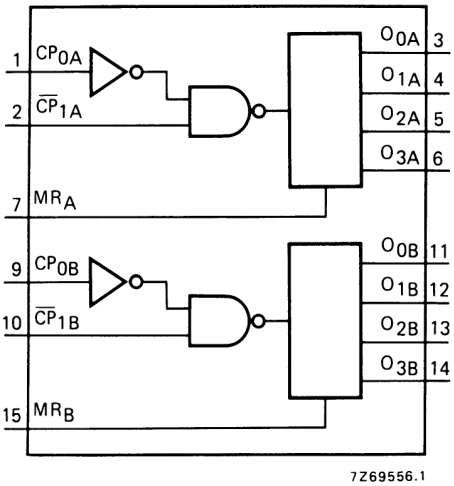


Fig. 1: The two counters inside 4520.(MR=master reset)

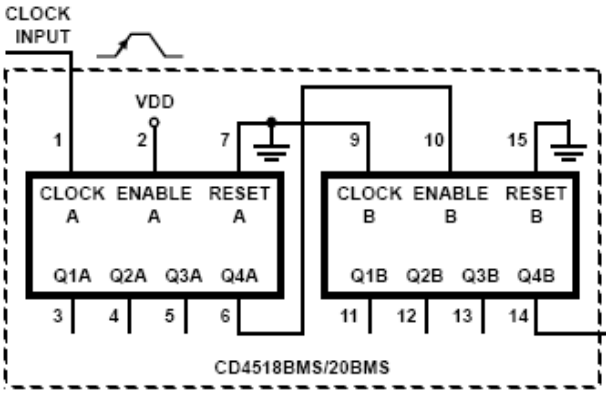


Fig. 2: Asynchronous 8-bit counter using both 4-bit counters in 4520.

In this diagram:
CLOCK=CP0 in Fig. 1
ENABLE=CP1 in Fig. 1
RESET=MR in Fig. 1

Q4B (pin 14) will see a 10Hz clock signal if the clock input is a 2560Hz clock signal.

The schematic shown in Fig. 2 is an asynchronous 8-bit binary counter made from cascading two 4-bit binary counters. This method of counting is asynchronous because the second 4-bit counter does not run on the same clock input; but instead indirectly run by the lowest frequency output of the first counter.

Step 3:
Use two 4510's (one for each BCD digit) to generate a two-digit decimal counting.

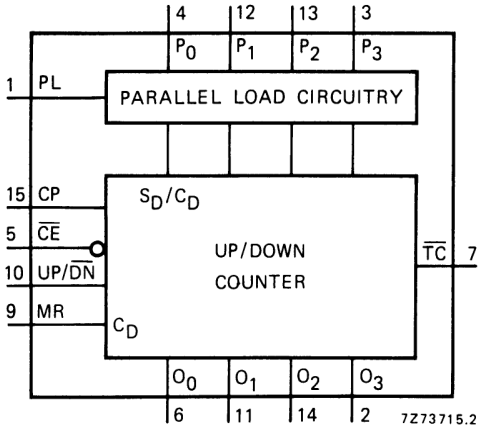


Fig. 3: Function diagram of 4510 BCD counter. This counter has the parallel load feature (P3-P0 and PL) so you can load the counter with a particular value on command. Connect PL to LOW to disable this feature.

We will use two 4510's to build a two-digit 00-99 decimal counter, by connecting the TC' (carry out, pin 7) output of the first stage (the lower digit) to the CE' (enable, pin 5) of the second stage (the higher digit). You may find an example at http://www.doctronics.co.uk/4510.htm. A link to this website can be found at the ELE202 course website.

Step 4:
You should verify your construction before moving on to the next lab. There are several possibilities: connect the counter outputs (one digit at a time) to the 4511 and then 7-seg display to verify the counting visually. You may also connect the 8 outputs (4 output or bits for each BCD digit) to 8 LEDs (don't forget about the resistors).

ELE202 Report Requirement
Lab 8 – BCD Counter

This is a full report submission:

- The report begins with a cover page. It should include the title of the lab, your name, your lab section, and the date the lab was submitted.
- Next, write a short abstract to summarize the lab – this should be 3 sentences or less.
- The main body of your report should include:
    1. The overall block diagram with rectangle boxes indicating counters, etc., at a higher abstractive view No detail connection is shown in this diagram. Do not draw an IC wiring diagram!
    2. Detail schematic of each step. Again do not use the IC wiring diagram (with the exception of perhaps the 555). Following the example of Fig. 2
    3. The formula of 555 and how you derive your Ra, Rb and C values.
- The last part of your report is a summary of:
    1. The obstacles and observations of the lab. Mention anything you do differently from what were described in this manual.
    2. Lesson learned.