CMOS Process

Polysilicon

$n^+$

$p^-$

$n^+$

$D^+$

$n$-well

$D^+$

$p$-substrate

$SiO_2$

Al
A Modern CMOS Process

Dual-Well Trench-Isolated CMOS Process
Its Layout View
The Manufacturing Process

For a great tour through the IC manufacturing process and its different steps, check
http://www.fullman.com/semiconductors/semiconductors.html
Typical operations in a single photolithographic cycle (from [Fullman]).
**Patterning of SiO2**

(a) Silicon base material

(b) After oxidation and deposition of negative photoresist

(c) Stepper exposure

Photoresist

SiO₂

Si-substrate

(d) After development and etching of resist, chemical or plasma etch of SiO₂

Hardened resist

SiO₂

Si-substrate

(e) After etching

(f) Final result after removal of resist

Chemical or plasma etch

Hardened resist

SiO₂

Si-substrate

Exposed resist

Patterned optical mask

UV-light
CMOS Process at a Glance

1. Define active areas
2. Etch and fill trenches
3. Implant well regions
4. Deposit and pattern polysilicon layer
5. Implant source and drain regions and substrate contacts
6. Create contact and via windows
7. Deposit and pattern metal layers
(a) Base material: p+ substrate with p-epi layer

(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask
CMOS Process Walk-Through

(d) After trench filling, CMP planarization, and removal of sacrificial nitride

(e) After n-well and $V_{Tp}$ adjust implants

(f) After p-well and $V_{Tn}$ adjust implants
(g) After polysilicon deposition and etch.

(h) After $n^+$ source/drain and $p^+$ source/drain implants. These steps also dope the polysilicon.

(i) After deposition of $\text{SiO}_2$ insulator and contact hole etch.
CMOS Process Walk-Through

(j) After deposition and patterning of first Al layer.

(k) After deposition of SiO$_2$ insulator, etching of via’s, deposition and patterning of second layer of Al.
Advanced Metallization
Advanced Metallization

Dual damascene IC process

- Oxide deposition
- Stud lithography and reactive ion etch
- Wire lithography and reactive ion etch
- Stud and wire metal deposition
- Metal chemical-mechanical polish

Source: IBM Corp.
Design Rules
3D Perspective

Polysilicon

Aluminum
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)
# CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
</tr>
</tbody>
</table>
Layers in 0.25 μm CMOS process

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>m1 m2 m3 m4 m5</td>
</tr>
<tr>
<td>well</td>
<td>nw</td>
</tr>
<tr>
<td>polysilicon</td>
<td>poly</td>
</tr>
<tr>
<td>contacts &amp; vias</td>
<td>ct v12,v23,v34,v45 nwc pwc</td>
</tr>
<tr>
<td>active area and FETs</td>
<td>ndif pdif nfct pfct</td>
</tr>
<tr>
<td>select</td>
<td>nplus pplus prb</td>
</tr>
</tbody>
</table>
Intra-Layer Design Rules

Same Potential
Well

Different Potential

Polysilicon

Metal1

Metal2

Active

© Digital Integrated Circuits 2nd Edition

© Digital Integrated Circuits 2nd Edition

Manufacturing
Transistor Layout
Vias and Contacts

1. Metal to Poly Contact
2. Metal to Active Contact
3. Via

Dimensions:
- 1
- 2
- 3
- 4
- 5

© Digital Integrated Circuits 2nd Manufacturing
Select Layer

Substrate

Well

Select

© Digital Integrated Circuits 2nd Edition

Manufacturing
CMOS Inverter Layout

(a) Layout

(b) Cross-Section along A-A’
Layout Editor
Design Rule Checker

poly_not_fet to all_diff minimum spacing = 0.14 um.
Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program
Packaging
Packaging Requirements

- **Electrical**: Low parasitics
- **Mechanical**: Reliable and robust
- **Thermal**: Efficient heat removal
- **Economical**: Cheap
Bonding Techniques

Wire Bonding

- Substrate
- Die
- Pad
- Lead Frame
(a) Polymer Tape with imprinted wiring pattern.

(b) Die attachment using solder bumps.
Flip-Chip Bonding

Solder bumps

Die

Interconnect layers

Substrate
Package-to-Board Interconnect

(a) Through-Hole Mounting

(b) Surface Mount
Package Types
## Package Parameters

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Capacitance (pF)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>68 Pin Plastic DIP</td>
<td>4</td>
<td>35</td>
</tr>
<tr>
<td>68 Pin Ceramic DIP</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>256 Pin Pin Grid Array</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>Wire Bond</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Solder Bump</td>
<td>0.5</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])
Multi-Chip Modules