Chapter 7  CMOS Amplifiers

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Chapter Outline

General Concepts

- Biasing of MOS Stages
- Realization of Current Sources

MOS Amplifiers

- Common-Source Stage
- Common-Gate Stage
- Source Follower
MOS Biasing

Voltage at X is determined by $V_{DD}$, $R_1$, and $R_2$.

$V_{GS} = -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1 \left( \frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH} \right)}$

$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}$

$V_{GS}$ can be found using the equation above, and $I_D$ can be found by using the NMOS current equation.
The circuit above is analyzed by noting M1 is in saturation and no potential drop appears across $R_G$. 

$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$
When in saturation region, a MOSFET behaves as a current source.

NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from $V_{DD}$ to a point (sources current).
Common-Source Stage

\[ \lambda = 0 \]

\[ A_v = -g_m R_D \]

\[ A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D R_D} \]

Input Applied to Gate

Output Sensed at Drain
In order to maintain operation in saturation, $V_{\text{out}}$ cannot fall below $V_{\text{in}}$ by more than one threshold voltage.

The condition above ensures operation in saturation.
CS Stage with $\lambda=0$

$A_v = -g_m R_L$

$R_{in} = \infty$

$R_{out} = R_L$
However, Early effect and channel length modulation affect CE and CS stages in a similar manner.

\[ A_v = -g_m \left( R_L \parallel r_O \right) \]

\[ R_{in} = \infty \]

\[ R_{out} = R_L \parallel r_O \]
Since $\lambda$ is inversely proportional to $L$, the voltage gain actually becomes proportional to the square root of $L$. 

$$|A_v| = \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L}}}{\lambda \sqrt{I_D}} \propto \sqrt[4]{\frac{2\mu_n C_{ox} WL}{I_D}}$$
To alleviate the headroom problem, an active current-source load is used. This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.

\[ A_v = -g_{m1} \left( r_{O1} \parallel r_{O2} \right) \]

\[ R_{out} = r_{O1} \parallel r_{O2} \]
PMOS CS Stage with NMOS as Load

\[ A_v = -g_{m2}(r_{O1} \parallel r_{O2}) \]

- Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.

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CS Stage with Diode-Connected Load

\[ A_v = -g_{m1} \frac{1}{g_{m2}} = \left( \frac{W/L_1}{W/L_2} \right) \]

\[ A_v = -g_{m1} \left( \frac{1}{g_{m2}} \parallel r_{o2} \parallel r_{o1} \right) \]

Lower gain, but less dependent on process parameters.
Note that PMOS circuit symbol is usually drawn with the source on top of the drain.

\[
A_v = -g_{m2} \left( \frac{1}{g_{m1} || r_{o1} || r_{o2}} \right)
\]
Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.

\[ A_v = - \frac{R_D}{1 + \frac{1}{g_m R_S}} \]

\[ \lambda = 0 \]
A diode-connected device degenerates a CS stage.

\[ A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \]
Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.

\[ V_{RG} = 0 \]
Output Impedance of CS Stage with Degeneration

Similar to the bipolar counterpart, degeneration boosts output impedance.

\[ r_{\text{out}} \approx g_m r_O R_S + r_O \]
Output Impedance Example (I)

When $1/g_m$ is parallel with $r_{o2}$, we often just consider $1/g_m$.

$$R_{out} = r_{o1} \left( 1 + g_{m1} \frac{1}{g_{m2}} \right) + \frac{1}{g_{m2}}$$
In this example, the impedance that degenerates the CS stage is \( r_o \), instead of \( 1/g_m \) in the previous example.

\[
R_{out} \approx g_m r_{o1} r_{o2} + r_{o1}
\]
Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.

\[ A_v = \frac{R_1 \parallel R_2}{R_G + R_1 \parallel R_2} \frac{-R_D}{1 + R_S} \frac{1}{g_m} \]

\[ A_v = -\frac{R_1 \parallel R_2}{R_G + R_1 \parallel R_2} g_m R_D \]
Common-gate stage is similar to common-base stage: a rise in input causes a rise in output. So the gain is positive.

\[ A_v = g_m R_D \]
In order to maintain $M_1$ in saturation, the signal swing at $V_{out}$ cannot fall below $V_b - V_{TH}$.
The input and output impedances of CG stage are similar to those of CB stage.

\[
R_{in} = \frac{1}{g_m}, \quad \lambda = 0, \quad R_{out} = R_D
\]
When a source resistance is present, the voltage gain is equal to that of a CS stage with degeneration, only positive.

\[ A_v = \frac{R_D}{\frac{1}{g_m} + R_S} \]
When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it (at low frequencies).

The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.

\[ R_{out} = (1 + g_m r_O) R_S + r_O \]
Example of CG Stage

Diode-connected $M_2$ acts as a resistor to provide the bias current.

\[
\frac{V_{out}}{V_{in}} = \frac{g_{m1} R_D}{1 + (g_{m1} + g_{m2}) R_S}
\]

\[
R_{out} \approx \left[ g_{m1} r_{o1} \left( \frac{1}{g_{m2}} \parallel R_S \right) + r_{o1} \right] \parallel R_D
\]
R₁ and R₂ provide gate bias voltage, and R₃ provides a path for DC bias current of M₁ to flow to ground.

\[
\frac{v_{out}}{v_{in}} = \frac{R₃ \parallel (1/g_m)}{R₃ \parallel (1/g_m) + R_S} \cdot g_m R_D
\]
Source Follower Stage

$A_v < 1$
Similar to the emitter follower, the source follower can be analyzed as a resistor divider.

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{r_O || R_L}{\frac{1}{g_m} + r_O || R_L}
\]
Source Follower Example

In this example, $M_2$ acts as a current source.

$$A_v = \frac{1}{g_{m1}} + r_{O1} \parallel r_{O2}$$
The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.

\[ R_{out} = \frac{1}{g_m} || r_O || R_L \approx \frac{1}{g_m} || R_L \]


- $R_G$ sets the gate voltage to $V_{DD}$, whereas $R_S$ sets the drain current.
- The quadratic equation above can be solved for $I_D$.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( V_{DD} - I_D R_S - V_{TH} \right)^2$$
If $R_s$ is replaced by a current source, drain current $I_D$ becomes independent of supply voltage.
Example of a CS Stage (I)

$A_v = -g_{m1} \left( \frac{1}{g_{m3}} \parallel r_{O1} \parallel r_{O2} \parallel r_{O3} \right)$

$R_{out} = \frac{1}{g_{m3}} \parallel r_{O1} \parallel r_{O2} \parallel r_{O3}$

- $M_1$ acts as the input device and $M_2$, $M_3$ as the load.
Example of a CS Stage (II)

- $M_1$ acts as the input device, $M_3$ as the source resistance, and $M_2$ as the load.

$$A_v = -\frac{r_{o2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}}} \parallel r_{o3}$$
Examples of CS and CG Stages

\[ A_{v_{cs}} = -g_{m2} \left[ (1 + g_{m1} r_{01}) R_S + r_{01} \right] || r_{01} \]

\[ A_{v_{cg}} = \frac{r_{02}}{\frac{1}{g_m} + R_S} \]

With the input connected to different locations, the two circuits, although identical in other aspects, behave differently.

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By replacing the left side with a Thevenin equivalent, and recognizing the right side is actually a CG stage, the voltage gain can be easily obtained.

\[ A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \]
Example of a Composite Stage (II)

- This example shows that by probing different places in a circuit, different types of output can be obtained.
- $V_{out1}$ is a result of $M_1$ acting as a source follower whereas $V_{out2}$ is a result of $M_1$ acting as a CS stage with degeneration.

$$
\frac{v_{out2}}{v_{in}} = -\frac{1}{g_m3} \parallel r_{03} \parallel r_{04}
= \frac{1}{g_m2} \parallel r_{02} + \frac{1}{g_m1}
$$