Delta-Sigma Modulators

Godi Fischer and Alan J. Davis
Dept. of Electrical & Computer Engineering
The University of Rhode Island
Kingston, RI, 02881-0805
U.S.A.
Tel.: + (401) 874 5879
Fax.: + (401) 782 6422
Email: fischer@ele.uri.edu

1 Introduction

Modulation can be defined as the systematic alteration of a carrier wave in accordance with a message (i.e. the information carrying signal). For example, in communications, modulation by a single frequency signal (carrier signal) allows a low frequency signal such as voice to be transformed into a narrow band signal at a high center frequency (with similar modulation returning the high frequency centered signal to its original form). Modulation of a signal by a periodic sequence of impulses (formally delta functions spaced uniformly in time) plays an important role in conversion of analog, time-varying signals into a digital format for storage, transmission, processing, coding, etc. In this case, the modulator replaces the continually varying signal by pulses, which correspond to sampled values of the analog signal in the time domain. This implies that the continually varying amplitude of the analog signal is approximated (or *quantized*) to a set of discrete signal levels. This discrete-time modulation is referred to as pulse code modulation (PCM). The Delta-Sigma ($\Sigma\Delta$) modulator is an offspring of the PCM family [1] and combines the quantization operation within a feedback loop configuration. In contrast to *conventional* PCM, which represents the sampled signal levels in form of multi-bit digital words, the $\Sigma\Delta$ modulator encodes the signal levels in the time domain by generating a corresponding sequence of (densely spaced) pulses. Hence, the modulator output, often limited to a single amplitude level (i.e., quantized to one bit), represents a pulse density modulated

(PDM) version of the input signal. Consequently, the original signal can be reconstructed (or demodulated) by time averaging, or lowpass filtering, this PDM signal. Due to the specific sequence of operations in the feedback loop configuration, the $\Delta\Sigma$ modulator sharply discriminates between the signal and the resulting quantization error. Despite the low number of output signal levels, this can provide a $\Delta\Sigma$ modulated signal with an extremely high dynamic range. $\Delta\Sigma$ modulators are therefore predominantly applied in high-resolution data conversion systems (e.g. systems with 12 or more bit resolution).

The basic $\Delta\Sigma$ modulator uses a feedback loop, which computes the difference between the instantaneous input signal and the previous (quantized) output (hence the name delta), followed by a (typically) discrete-time integrator or accumulator (denoted by the symbol sigma). The actual modulator output is a coarsely quantized version of the integrator output signal. Figure 1 shows a simplified block diagram of a single integrator or first-order $\Delta\Sigma$ modulator loop. If the input is a digital signal, the $\Delta\Sigma$ modulator can be realized using digital signal processing only and the digital-to-analog converter (DAC), shown by dashed lines in figure 1, is not required. In the special case of a 2-level or 1-bit quantizer, the DAC reduces to a simple voltage or current reference, which provides the appropriate analog signal levels $\pm V_{ref}$ or $\pm I_{ref}$, respectively.

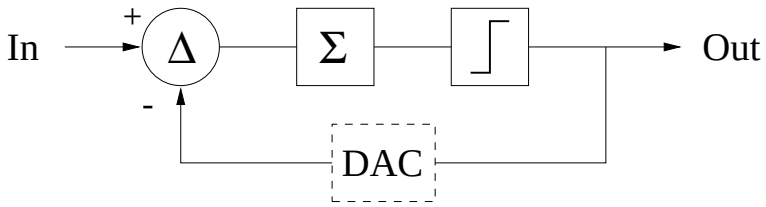

Figure 1: Block diagram of first-order $\Delta\Sigma$ modulator, consisting of a difference stage Δ, an integrator Σ, a (coarse) quantizer and (possibly) a D/A converter in the feedback path.

Like its older cousin, the delta modulator [2], the $\Delta\Sigma$ modulator employs oversampling and feedback to allow coarse quantization while preserving a small in-band noise level. The major difference between these two techniques lies in the positioning of the integrator within the modulator loop. While the delta modulator places the integrator into the feedback path, the $\Delta\Sigma$ modulator integrates the signal prior to the quantization process. Consequently, the delta modulator generates a differentiated (or highpass filtered) version of the input signal while the $\Delta\Sigma$ modulator, by differentiating *and* integrating in the forward path, passes the signal essentially unchanged through the system. Therefore, the output of the $\Delta\Sigma$ modulator contains a precise, albeit quantization noise corrupted,

replica of the input signal. Since the negative feedback inherently differentiates the quantization error sequence, the corresponding noise spectrum is highpass filtered, with little quantization noise overlapping the low frequency signal spectrum. This spectral discrimination between signal and noise, also referred to as noise shaping, is a unique property of $\Delta\Sigma$ modulators. Depending on the relative signal bandwidth, this feature enables an extremely wide dynamic range and explains the popularity of the $\Delta\Sigma$ approach in the field of high resolution data conversion.

$\Delta\Sigma$ based data converters can be found in many of today's commercial communication products. A common feature of all applications is the objective of high-resolution (e.g. 12 bit or more). Due to the required oversampling ratio (OSR), defined as sampling rate divided by twice the signal bandwidth, the conversion speed is rather moderate (typically below 1MHz). An important reason for the frequent use of $\Delta\Sigma$ modulators in high-resolution data converters is their comparatively low implementation cost, which is a consequence of the insensitivity of the modulator performance with respect to minor element ratio deviations. This eliminates an expensive component trimming procedure and paves the way for a completely monolithic implementation using standard CMOS technology.

Digital telephony provides many opportunities for the application of $\Delta\Sigma$ modulators [3]. There exist many subsets in this field with varying requirements such as voiceband codecs for the public switched telephone networks (requiring 13 bit linear resolution), echo-canceling modems (with 12-16 bit resolution) or Integrated Service Digital Network (ISDN) interface transceivers (with 13-16 bit resolution). Digital cellular phones utilize $\Delta\Sigma$ modulators both for voiceband speech coding and for IF-to-baseband radio interface data conversion. Another field most readers will be familiar with is digital audio. With 14-18 bit resolution for consumer grade equipment and up to 4 times as much precision for professional audio equipment, no other conversion technique can seriously compete with the $\Delta\Sigma$ approach as far as the cost/resolution ratio is concerned. A third area where $\Delta\Sigma$ modulation has achieved prominence is in sonar signal processing, particularly in beamforming applications. Due to the high element count in sonar arrays, power efficient and compact analog-to-digital converters (ADC's) are of paramount importance. Finally, there is the field of metrology with its ever increasing demand for more precision. Since most measurement systems acquire the raw data in analog form while the subsequent data processing is carried out in the digital domain, there exists a high demand for precise data conversion. $\Delta\Sigma$ modulation is likely to assume a prominent role in this field as well.

The large majority of today's commercially available $\Delta\Sigma$ ADC's are realized by switched capacitor (SC) techniques, a fully CMOS compatible discrete-time analog circuit design technique [4]. A few ADC implementations employ switched current (SI) circuits, the alternative (CMOS compatible) discrete-time analog technique.

As technology continues to advance, a variety of other fields are likely to be influenced by the advent of $\Delta\Sigma$ modulation. Chief among the new areas will be video and image coding applications. This field will require system sampling rates beyond 100 MHz, a range that is within reach of contemporary silicon technology. Apart from improving the existing silicon implementations by gradually increasing resolution and/or conversion rates, some researchers have begun to investigate the possibility of applying the $\Delta\Sigma$ approach to an altogether different fabrication technology such as circuits realized by super-conducting devices [5]. If successful, these efforts will enable additional applications, particularly those involving very high frequency signals.

2 Basic Concepts

The most prominent feature of a $\Delta\Sigma$ modulator is its capability to shape the quantization noise, as explained in the following subsection. We then derive a simple parametric expression for the modulator output noise power. The last subsection reveals how the noise shaping concept is utilized as a key element in high-resolution data conversion systems.

2.1 Noise Shaping

Modulation is an inherently nonlinear process. This considerably complicates the modulator analysis. In fact, there exists no rigorous mathematically treatment that allows the designer to predict the exact behavior of a $\Delta\Sigma$ modulator under all practical operating conditions. In lieu of a better alternative, we adopt the frequently applied technique of describing the modulator by a linearized model, whereby the nonlinear quantizer is replaced by an additive (white) noise source. Such a model is sufficient to explain the most fundamental characteristic of a $\Delta\Sigma$ modulator, namely the shaping of the quantization noise. It is also capable of estimating the performance of a wide variety of modulator architectures. However, the linear model breaks down when we ponder questions related to stability. At present, stability issues and other nonlinearity related problems such as

the occurrence of spurious passband tones have to be dealt with on an ad hoc basis or, alternatively, by evoking a numerical simulator, which closely mimics the modulator's behavior in the time domain, such as the program DelSi [6].

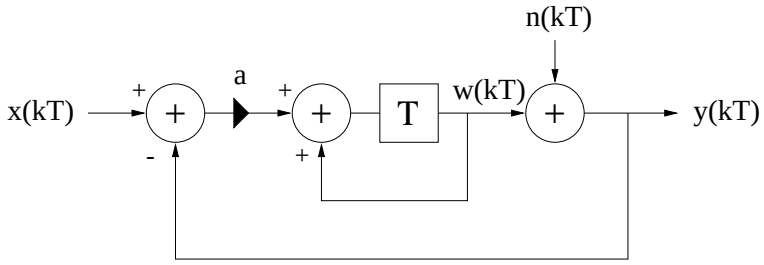

Figure 2: Block diagram of a discrete-time linearized first-order $\Delta\Sigma$ modulator with an integrator scaling factor a.

Figure 2 shows a linearized, discrete-time model of the first-oder (or single integrator) $\Delta\Sigma$ modulator. The quantizer has been replaced by an additive noise source and the accumulator (sigma) has been modeled as a forward difference (or forward Euler) integrator. For the ideal un-scaled case (i.e., $a = 1$), this first-order system is governed by the following difference equations

$$w([k+1]T) = \quad w(kT) + x(kT) - y(kT) \tag{1}$$

$$y(kT) = \qquad w(kT) + n(kT) \tag{2}$$

T represents the cycle time of the sampling frequency, which, for the sake of convenience, is often equated to unity and not explicitly listed as an argument. Transforming this equation set into the z-domain yields

$$W(z) = \quad [W(z) + X(z) - Y(k)]z^{-1} \tag{3}$$

$$Y(z) = \qquad W(z) + N(z) \tag{4}$$

Finally, by using (4) to eliminate W(z) in (3) and solving for Y(z), we obtain

$$Y(z) = X(z)\ z^{-1} + N(z)\ [1 - z^{-1}] \tag{5}$$

This result shows that the modulator output $Y(z)$ consists of a delayed but otherwise intact version of the input signal $X(z)$ plus an additive, digitally differentiated term representing the quantization error. We deduce from equation (5) that $\Delta\Sigma$ modulators

can generally be represented by two transfer functions: a signal transfer function (STF) defined as the ratio Y/X (in the absence of noise) and a noise transfer function (NTF) defined as the quotient Y/N (in the absence of an input signal).

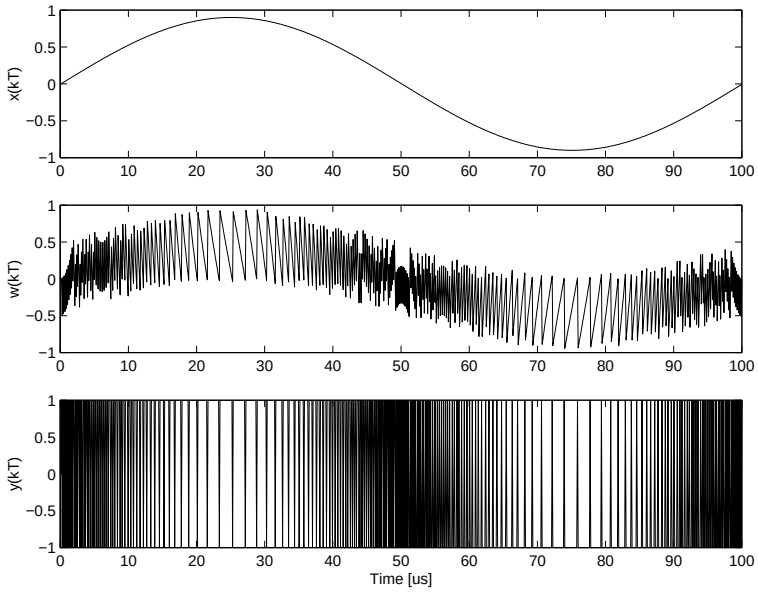

Figure 3: Spectral response of first-order $\Delta\Sigma$ modulator to a 10 kHz sinusoidal input signal (DelSi simulation with $f_s = 10$ MHz).

Figure 3 depicts the time domain response of the first-order system to a 10 kHz sinusoidal input signal. We have normalized the two quantizer output levels in this DelSi simulation to ± 1 while the sampling rate has been set to 10 MHz. The plot shows the input signal (top trace), the integrator output (center curve) and the final $\Delta\Sigma$ modulated output (bottom trace). In order to limit the output swing of the noisy integrator to the depicted range of ± 1, a scaling factor $a = 0.5$ was used. For this more general case with $a \neq 1$, equation (5) changes to

$$Y(z) = X(z)\,\frac{az^{-1}}{1 - z^{-1}[1-a]} + N(z)\,\frac{1 - z^{-1}}{1 - z^{-1}[1-a]} \tag{6}$$

By choosing $a < 1$, we have actually modified the loop gain and with it the position of the only pole of the system. It moved from the z-domain origin (z=0) to the positive real value $[1 - a]$. The output of the scaled loop still comprises the same two signal components. This time, however, the input signal is spectrally shaped by a first-order lowpass filter while the NTF becomes a highpass filter rather than an ideal differentiator.

Since the lowpass filter yields unity gain in the passband, the finite pole does not corrupt the signal as long as the signal energy resides within that band. The passband gain of the NTF, however, has been enhanced by a factor of $1/a$. Fortunately, this noise gain is neutralized by a corresponding reduction of the quantization error. The quantization error is defined as the difference between the quantizer input and output signal. Hence, scaling the quantizer input by $a < 1$ reduces the quantization error, which in turn neutralizes the increased noise gain. The noise shaping property is therefore not affected by this scaling procedure.

The presented linearized analysis procedure served well to explain the noise shaping property and, as will be seen, provides useful design guidelines and an efficient means to estimate the modulator performance. However, it fails to explain some of the more subtle non-ideal features of $\Delta\Sigma$ modulators such as the occurrence of passband tones or the potential instability of higher order loops. For a more rigorous mathematical treatment of quantization noise related questions in single-loop $\Delta\Sigma$ modulators, the interested reader is referred to [7].

2.2 Output Noise Power

A crucial parameter for the assessment of the modulator performance is the total output noise power, or, in presence of a deterministic input signal, the corresponding signal-to-noise ratio (SNR).

Provided the quantization error represents the dominant system noise source, we can compute the total mean square in-band noise at the output of the modulator loop as follows:

$$n_o{}^2 = e_q{}^2 \, \frac{2}{f_s} \int_0^{BW} \mid NTF \mid^2 df \tag{7}$$

where $e_q{}^2$ represents the mean square quantization error, f_s the applied sampling rate and BW the effective signal bandwidth. By normalizing all frequency related terms in (7), (i.e., f_s, BW and df) to the oversampling rate $OSR = f_s/2BW$, we can reduce the dependency of the output noise power to three parameters: the mean square quantization error $e_q{}^2$, the modulator OSR and the squared magnitude of the NTF.

If we expand the first-order modulator (cf. figure 1) to an m^{th} order system by replacing the single integrator with a cascade of m identical cells, the un-scaled z-domain NTF becomes $[1 - z^{-1}]^m$. Using $z = e^{j2\pi f/f_s}$ and employing Euler's formula for the sine

function, we can rewrite the squared magnitude of the m^{th} order NTF in the frequency domain as

$$\mid NTF_m(f) \mid^2 = [2\ sin(\pi f/f_s)]^{2m} \tag{8}$$

Furthermore, since $f/f_s \ll 1$ in the passband region of the modulator, we can approximate the sine function by its argument $(\pi f/f_s)$. The in-band noise power present at the output of an ideal m^{th} order modulator (including the case m=1) can thus be written as

$${n_{om}}^2 = {e_q}^2\ \frac{\pi^{2m}}{2m+1}\ OSR^{-[2m+1]} \tag{9}$$

Apart from the actual quantization error e_q, the output noise power strongly depends on the OSR and the system order, or integrator multiplicity, m. For example, adding one more integrator to the modulator loop reduces the output noise power by approximately a factor of $(OSR/\pi)^2$. Likewise, doubling the OSR suppresses the noise by an additional factor of $2^{[2m+1]}$. Both values manifest a very significant noise reduction.

2.3 A/D and D/A Conversion

With the above background, we next consider $\Delta\Sigma$ modulation with analog input signals in more detail. Consider the sample curves depicted in figure 3 for a first-order modulator. The bottom trace, the modulator output, consists of a dense sequence of clock synchronized pulses, which are restricted in amplitude to the two levels ± 1 (e.g. corresponding to voltage levels $\pm V_{ref}$). This constitutes the digital output of the $\Delta\Sigma$ modulator. The signal information (a sine function in figure 3) resides in the density of the pulses, which, for sufficiently small time granularity (i.e. high oversampling rate), provides an accurate coding of the input signal. The input signal can be reconstructed from the modulator output either in the analog domain (by time averaging the discrete pulse train via an analog lowpass filter) or in the digital domain (by down-sampling or decimating using a digital lowpass filter and re-sampling at the Nyquist rate $f_s{}^*2BW$). Figure 4 illustrates two distinct converter systems, each comprising a $\Delta\Sigma$ modulator as its centerpiece, but one serving as an ADC and the other as a DAC.

Although two out of the three cells in the ADC system in figure 4 (top) are analog, the main burden of the implementation cost falls onto the digital side. Due to oversampling, the anti-alias filter specifications are very relaxed. Therefore, the pre-filter can be emulated by a low order lowpass circuit. By contrast, the digital lowpass/decimation

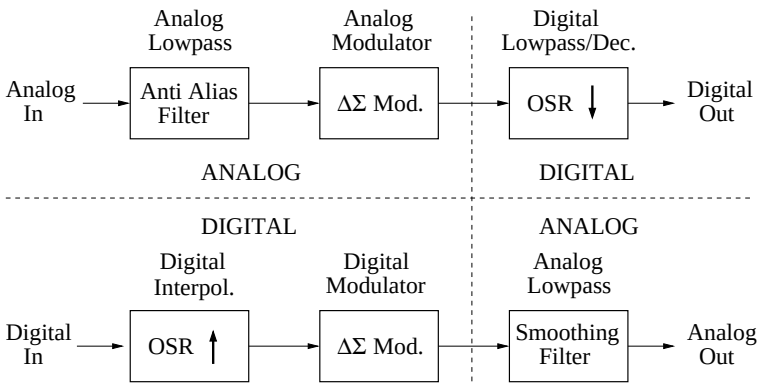

Figure 4: Block diagram of a complete $\Delta\Sigma$ based A/D (top) and D/A converter system (bottom).

stage may be a complex filter system with a very narrow transition band that becomes smaller relative to the sampling rate (or the OSR). Its implementation is therefore costly and requires a significant amount of silicon real estate. For example, realizing the low-pass/decimator by a single-stage FIR filter may require a delay line with as many as 4,000 taps [8]. Fortunately, the data path at the filter input is rarely more than a few bits wide. Furthermore, the down-sampling process reduces the computation rate by almost a factor of OSR, which in turn enables a very compact hardware implementation. The DAC implementation, finally, with the smoothing filter as its only analog cell, is a predominantly digital system.

The growing popularity of the $\Delta\Sigma$ approach is part of an ongoing digital revolution that not only affects micro-electronics but also many of its adjacent fields, most prominently computers and communications. As figure 4 illustrates, the $\Delta\Sigma$ approach reflects this trend very well by allowing a larger percentage of the total implementation cost to be paid in *digital currency*. Despite this digital dominance, the system performance continues to be tightly linked to the performance of the few remaining analog cells, i.e., the modulator loop in case of an ADC implementation or the smoothing filter in a DAC realization.

3 Modulator Architectures

Good design is characterized by a well-balanced compromise between system performance and implementation cost. In the context of $\Delta\Sigma$ modulation, we equate performance to

a weighted sum of dynamic range (or resolution) and signal bandwidth (or conversion rate). The cost function comprises parameters such as circuit complexity (silicon real estate, power), modulator robustness (non-ideal effects, yield) and required OSR (power, signal bandwidth). The following section considers the performance versus cost trade-offs that exist among the most frequently applied modulator architectures.

Equation (9) provides an ideal starting point for our investigation. It describes the output noise power of an (ideal) m^{th} order modulator as a function of the three characteristic parameters mean square quantization error ${e_q}^2$, required OSR and system order m. Accordingly, one can minimize the modulator output noise in three ways.

The first solution aims at reducing the quantization error power ${e_q}^2$ at its very origin. This can be achieved by replacing the typical 2-level (1-bit) quantizer at the modulator output with a multi-level quantizer. For instance, trading the 1-bit quantizer for a ternary system (with signal levels ± 1 and 0) already reduces the noise power by a factor of 4. Apart from increasing the dynamic range of the converter, this measure also linearizes all intermediate signals inside the modulator loop. Consequently, a multi-level system is less likely to suffer from nonlinear effects such as limit cycles and residual inter-modulation products, which give rise to spurious tones in the modulator passband. The major drawback of this solution is the extremely high linearity requirement for the DAC located either in the feedback path of the modulator (in case of an ADC implementation) or in front of the smoothing filter (for a DAC realization). In contrast to errors stemming from the quantizer in the forward path, nonlinear effects occurring in the feedback branch of the modulator are not noise shaped. Consequently, they v'can severely limit the system performance. Since component trimming is not an option in a monolithic implementation, the designer is left with two possible remedies. The first one is to apply an adaptive error correction algorithm, which automatically compensates for the encountered nonlinearities [9]. The second measure is based on the principle of dynamic element matching [10]. This technique presumes that the p output levels of the DAC are realized by p identical unit elements (e.g. capacitors or current sources). These elements are then selectively switched in parallel such that their sum corresponds to the desired output level, while the switch selection algorithm time-averages (or lowpass filters) the conversion error sequence. An efficient solution for such a spectral shaping of DAC errors is presented in [11].

The second solution for improving the modulator noise shaping characteristic is to increase the OSR. This measure is simple and effective, but it severely limits the signal bandwidth (for given sampling rate) or else requires a correspondingly higher sampling

rate (for given signal bandwidth). In this context, it is important to recall that the corresponding resolution versus bandwidth trade-off is highly nonlinear. For instance, doubling the OSR of a 3^{rd} order system, while maintaining the sampling rate, can increase the dynamic range by as much as 21 dB (or more than 3 bits). The bandwidth, on the other hand, will be reduced by a mere factor of 2.

In many implementations, the OSR does not constitute an integral part of the modulator architecture and remains a free parameter. This allows the user to trade-in bandwidth for resolution even after device fabrication (provided the pre- and post-filters flanking the modulator cell support this kind of flexibility).

In the third approach, the noise shaping efficiency is improved by increasing the order of the modulator loop filter. Unfortunately, simply inserting m integrators into the forward path of the modulator does not yield a stable solution if m exceeds two. This instability can be traced back to the spectral shape of the ideal (z-domain) differentiator function. At very low frequencies, where $z \approx 1$, the term $(1 - z^{-1})^m$ approaches zero and suppresses the noise correspondingly. At high frequencies however, where $z \approx -1$, the gain of the m^{th} order differentiator approaches 2^m. This increase in the gain of high frequency noise can exceed the modulator's noise tolerance and render the system unstable. There exist two practical solutions to this problem. In the first case, the single modulator loop is replaced by a multi-stage configuration, which consists of stable first and/or second-order modules only. Each additional stage creates an estimate of the quantization noise of its predecessor. This noise estimate is subsequently (digitally) subtracted from the output of the previous stage. This approach was first proposed for delta modulation and was later expanded to delta-sigma modulation [12]. This implementation is known as a cascade encoder or multi-stage modulator. As an additional benefit, the correlated noise subtraction of the multi-stage solution whitens the quantization noise spectrum and so prevents the occurrence of spurious tones. However, noise reduction by subtraction requires well matched element ratios (e.g. capacitors or current mirrors) in the analog modulator loop and typically high op-amp open-loop gains to avoid integrator pole shifts, which otherwise cause leakage.

In the alternative high-order solution, the original cascade of m integrators is complemented by additional feedback paths, which enable the designer to precisely control the placing of the system poles. With properly placed poles, it is possible to obtain a conditionally stable solution. Similar to the multi-stage approach, the multiple feedbacks of the modified system tend to de-correlate the quantization error from the input signal and

thus whiten the noise spectrum. In contrast to the multi-bit solution, however, high-order single-bit modulators preserve the insensitivity of single-bit low-order circuits with respect to minor variations of the analog component values. The major obstacle in this case is the difficulty of designing these high-order loops such that stability can be guaranteed under the typical operating conditions. Since stability is a mandatory condition for any practical system, this issue has been thoroughly researched during the late 1980's and early 1990's. Although an unconditionally stable solution or a comprehensive stability analysis procedure for $m \geq 3$ has not yet been found, numerical optimization techniques have enabled several successful circuit implementations (e.g. [13], [14]). As a matter of fact, most of today's commercial $\Delta\Sigma$ type ADC's are based on single-stage high-order modulator topologies.

The following two subsections present four of the most widely used modulator topologies. They are separated into two categories, termed multi-stage and single-stage modulators.

3.1 Multi-stage Modulators

The two most frequently applied multi-stage topologies are the triple cascade of first-order modulators, referred to as MASH [15], and the cascade of a second-order and a first-order (SOFO) modulator [16]. The two architectures are illustrated by their respective block diagrams in figure 5 and figure 6. If we simplify the z-domain analysis by replacing the denominator function of each modulator stage by its dc value, we can describe the MASH modulator by the following equation set

$$
\begin{aligned}
Y_1(z) = &\quad X(z)z^{-1} + N_1(z)(1 - z^{-1}) && (10)\\
N_1(z) = &\quad Y_1(z) - W_1(z)\tfrac{1}{a_1} && (11)\\
Y_2(z) = &\quad -N_1(z)z^{-1} + N_2(z)(1 - z^{-1}) && (12)\\
N_2(z) = &\quad Y_2(z) - W_2(z)\tfrac{1}{a_2} && (13)\\
Y_3(z) = &\quad -N_2(z)z^{-1} + N_3(z)(1 - z^{-1}) && (14)
\end{aligned}
$$

In order to eliminate the in-band quantization noise contributions N_1 and N_2 of the first and second stage, respectively, the following digital noise cancellation (digital filter) can be applied

$$\begin{aligned} Y(z) = &\quad Y_1(z)z^{-2} + Y_2(z)z^{-1}(1-z^{-1}) + Y_3(z)(1-z^{-1})^2 \\ = &\quad X(z)z^{-3} + N_3(z)(1-z^{-1})^3 \end{aligned} \tag{15}$$

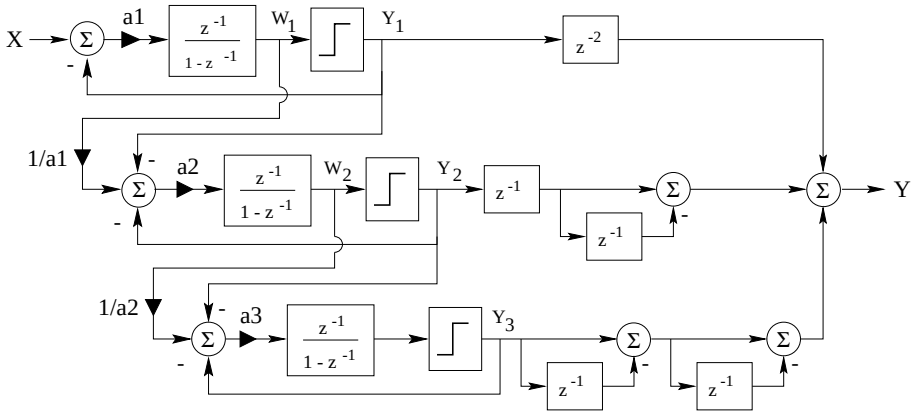

Figure 5: Triple first-order cascade or MASH modulator topology with corresponding digital noise cancellation circuit.

The dominant remaining in-band noise term after this operation is the triple differentiated quantization noise introduced by the 3^{rd} (or last) stage. The total output noise power of the ideal MASH can therefore be computed as indicated by equation (9) when setting $m = 3$.

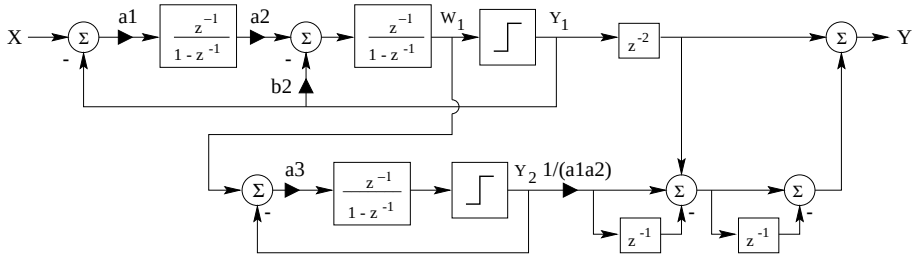

Figure 6: Cascade of a second-order first-order modulator with corresponding digital noise cancellation scheme.

The SOFO circuit depicted in figure 6 has been slightly modified from its originally proposed version [17]. The block diagram shows no signal path between the quantized first stage output and the second stage input. While this simplifies the analog implementation,

it requires a slightly more complex digital noise cancellation procedure. Applying the previous analysis procedure to the SOFO yields the following equation set

$$\begin{aligned} Y_1(z) = &\quad X(z)z^{-2} + N_1(z)(1-z^{-1})^2 && (16)\\ N_1(z) = &\quad Y_1(z) - W_1(z)\,\tfrac{1}{a_1 a_2} && (17)\\ Y_2(z) = &\quad W_1(z)z^{-1} + N_2(z)(1-z^{-1}) && (18) \end{aligned}$$

The first stage noise contribution, N_1, is eliminated by the following procedure

$$\begin{aligned} Y(z) = &\quad Y_1(z)z^{-1} - Y_1(z)z^{-1}(1-z^{-1})^2 + Y_2(z)\tfrac{1}{a_1 a_2}(1-z^{-1})^2 \\ = &\quad X(z)z^{-3} + N_2(z)\tfrac{1}{a_1 a_2}(1-z^{-1})^3 \qquad (19) \end{aligned}$$

Obviously, the SOFO modulator is not as efficient a noise shaping circuit as the MASH. According to our simple linear analysis, the difference in noise suppression is equal to the product of the two forward coefficients in the first stage of the SOFO cascade, i.e., $a_1 a_2$. A practical value of this product is $\frac{1}{4}$. Hence, the difference in noise suppression should amount to approximately 12 dB. To confirm this result, we have carried out a DelSi simulation with both topologies. In so doing, we have assumed a 20 kHz sinusoidal input signal of 0.707 V amplitude (i.e., -6 dB relative power) and a sampling rate of 10 MHz. The simulation results are displayed in figure 7. To reduce the variance of the noise, the two output spectra (solid line for MASH, dotted line for SOFO) have been computed by averaging two 2^{16} point FFT's. The plot reveals an average noise power difference between the two curves of approximately 10 dB. This agrees well with the theoretical prediction derived from the crude linear models.

The monotonically increasing noise floors in figure 7 reveal further that both topologies allow the designer to treat the OSR as a free parameter. Table I illustrates some possible trade-offs between OSR, signal bandwidth (BW) and maximum SNR.

Despite the excellent noise shaping capability of the MASH topology, an analog designer may be reluctant to utilize this solution since the superior performance implies a perfect noise cancellation that will be difficult to achieve with practical circuits. Due to amplifier non-idealities and the inherent parametric variations of micro-fabricated devices, this is not possible. The two main problems confronting the designer are integrator leakage (caused by a shift of its pole) and coefficient mismatch (due to statistical process variations). Integrator leakage is particularly severe because it adds an additional parasitic term to the ideal m^{th} order NTF of the form

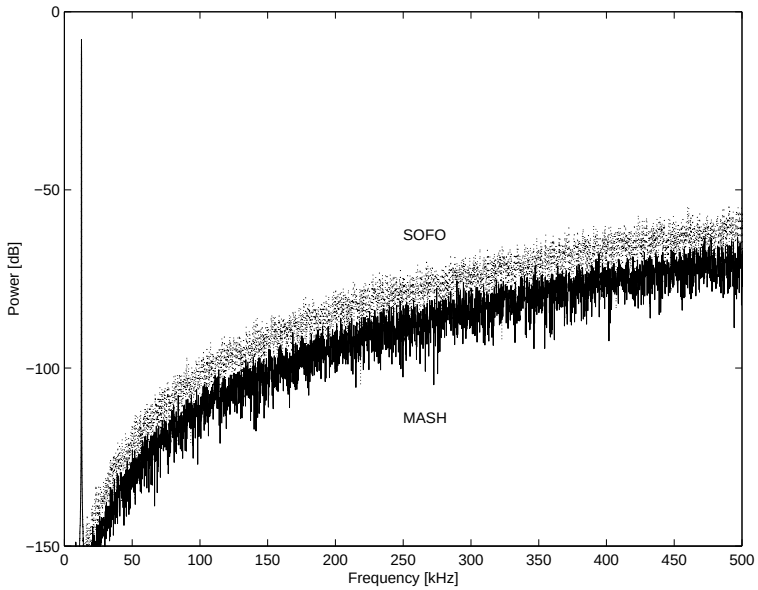

Figure 7: Frequency spectrum of MASH (solid line) and SOFO modulator (dotted line) in presence of a 20kHz sinusoidal input signal (DelSi simulation with $f_s = 10$ MHz).

$$NTF(z)_{m_{actual}} \approx NTF(z)_{m_{ideal}} + \epsilon_{leak}\ (1 - z^{-1})^{[m-1]} \tag{20}$$

where ϵ_{leak} denotes the magnitude of the integrator leakage term. Even though leakage affects both of the presented topologies, its effect is more pronounced in the MASH case since the leakage term of its first integrator is not noise shaped at all. In the SOFO implementation, the first stage is a second-order circuit, yielding a first-order noise shaped leakage term. Consequently, its contribution to the total output noise power will be on the order of $(OSR/\pi)^2$ smaller than the parasitic first-stage contribution of the MASH.

Similar reasoning can be applied to the ratio mismatch problem with the notable exception that ratio matching errors stemming from an m^{th} order circuit are m^{th} order noise shaped. Therefore, ratio (or integrator gain) errors weigh approximately a factor $(OSR/\pi)^2$ less heavily than integrator leakage terms.

For a more detailed discussion regarding parasitic effects in SC based modulator circuits, the reader is referred to [18].

3.2 Single-stage Modulators

Most single-stage modulators can be derived from two basic topologies. The two architectures have originally been referred to as noise-shaping coders of form I and form II, respectively [19]. This nomenclature indicates that they form a transpose pair. In classical filter theory, the corresponding two feedback arrangements are called follow-the-leader feedback (FLF) and inverse follow-the-leader feedback (IFLF). In what follows, we will refer to them by the latter two acronyms. The block diagrams of the FLF and the IFLF topology are displayed in figure 8 and figure 9, respectively. Note that both diagrams exhibit an additional feedback path, i.e., b_4, which leap-frogs two integrator stages. This extra feedback loop significantly improves the quantization noise suppression by placing a finite zero into the stopband of the NTF. This zero insertion technique requires the cascade of integrators to consist of alternating backward and forward Euler equivalent functions. Since the passband zero is located near the frequency origin (where z=1), the corresponding zero loop gain becomes very small. The finite zero loop thus hardly affects the STF and can be ignored in the initial pole placement procedure.

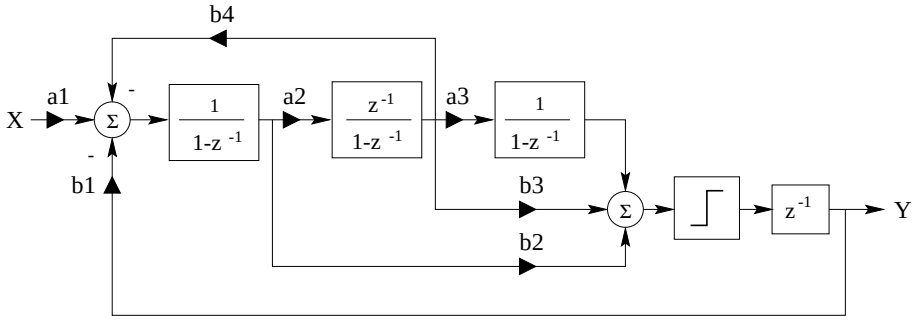

Figure 8: Single-stage 3^{rd} order modulator in FLF topology with additional feedback path b_4 yielding a finite NTF zero.

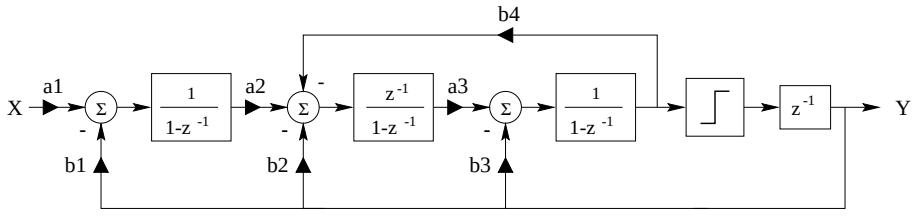

Figure 9: Single-stage 3^{rd} order modulator in IFLF topology with additional feedback path b_4 realizing a finite NTF zero.

By minimizing the magnitude of the NTF (in the mean square sense) over the entire modulator passband, we obtain the following analytic expression for the optimum zero loop gain G_{z_3} of a 3^{rd} order system

$$G_{z_3} = \frac{3}{5}\,\frac{\pi^2}{OSR^2} \tag{21}$$

If we include the above expression in our linear circuit analysis procedure, we can approximate the total noise power at the output of a 3^{rd} order FLF or IFLF modulator by

$$n_{03_{FLF/IFLF}} \approx e_q^2\,\frac{1}{(b_1 a_2)^2}\,\frac{4}{25}\,\frac{\pi^6}{7}\,OSR^{-7} \tag{22}$$

This approximation features two additional quantities, which do not appear in the generic expression of equation (9), namely the squared coefficient product $(b_1 a_2)^2$ due to the pole placement and the fraction 4/25 introduced by the finite NTF zero. The maximum value of the coefficient product is dictated by stability considerations and lies somewhere between 0.06 and 0.08. It is interesting to note that the zero loop gain G_{z_3} scales as the inverse square of the OSR while the resulting additional noise suppression factor remains constant. This observation also applies to higher order circuits which may possess more than just one passband zero.

If we replace the coefficient product $(b_1 a_2)$ in equation (22) by a typical value of, say 0.07, we deduce that 3^{rd} order FLF or IFLF modulators realize approximately 30 times (or 15 dB) less noise suppression than an ideal 3^{rd} order noise shaped modulator (cf. equation (9)). Since this numerical value has been derived from the simple linear modulator model, it requires further verification. To do so, we have performed studies using the service of our behavioral simulator DelSi. All simulations have been carried out with a 20 kHz sinusoidal input of 0.707 V amplitude and a sampling rate of 10 MHz. In each case, the noise power has been computed via a 2^{16} point FFT. The results are summarized in table I.

OSR	BW	SNR_{MASH}	SNR_{SOFO}	$SNR_{(I)FLF}$
32	156 kHz	83 dB	73 dB	72 dB
48	104 kHz	95 dB	86 dB	83 dB
64	78 kHz	105 dB	95 dB	93 dB
96	52 kHz	117 dB	107 dB	105 dB
128	39 kHz	126 dB	115 dB	114 dB

Table I. Signal bandwidth and maximum SNR versus OSR for the SOFO, the MASH and the 3^{rd} order FLF/IFLF architecture. The listed values are DelSi results obtained with $f_s = 10$ MHz).

The SNR values listed in table I are in good agreement with equation (9), which predicted a 21 dB reduction of the output noise power for every doubling of the OSR. Although all topologies yield essentially the same SNR improvement as the OSR increases, the reader should bear in mind that the non-monotonic shape of the NTF of high-order single-stage modulators requires a physical adjustment of the zero frequency, i.e. the loop gain factor G_{z_3}, as indicated by equation (21).

As far as the efficiency of the noise suppression is concerned, FLF/IFLF circuits are inferior to their multi-stage counterparts, above all to the MASH topology, which closely approaches the theoretical maximum expressed by equation (9). On the other hand, single-stage circuits exhibit the highest tolerance with regard to non-ideal effects such as integrator leakage or coefficient mismatch. This renders them very attractive for ADC implementations, where the modulator cell is realized by analog means (cf. figure 4). Finally, it is important to recall that only single-stage topologies can realize the desired simple 1-bit output format. The digital noise cancellation procedure in multi-stage circuits invariably creates a multi-bit output by differentiating and summing several 1-bit signals. This last property is probably the most important reason for the popularity of the single-stage approach in commercial $\Delta\Sigma$ ADC circuits.

4 Design Example

This last section presents a simple ADC design example. We assume the converter to be intended for a signal bandwidth of 100 kHz or, equivalently, a Nyquist conversion rate of 200 kHz. A typical resolution for such an extended audio or sonar application is 14-16 bit. To minimize the implementation cost for the digital decimator, we require a simple 1-bit

output format. Finally, to keep the total power dissipation low, we impose a maximum OSR of 32. This mandates a minimum modulator sampling rate of 6.4 MHz.

The above specifications require a minimum system order of five. Among the two competing single-stage topologies, we have chosen the IFLF implementation, because it requires no additional analog summing stage (cf. figure 8). The block diagram of the 5^{th} order IFLF circuit, called IFLF5, is shown in figure 10. Apart from the two additional feedbacks b_6 and b_7, which realize two finite passband zeros, the depicted IFLF topology also features a second feed-in path, i.e., a_{31}. This second input enables the designer to compensate for a possible excess signal gain in the vicinity of the system poles by placing an additional zero into the STF. Although the poles are located outside the modulator passband, an excess signal gain can trigger additional nonlinear effects, which in turn can significantly reduce the maximum input swing. Since the additional feed-in path does not form any loop, the NTF is not affected by this measure.

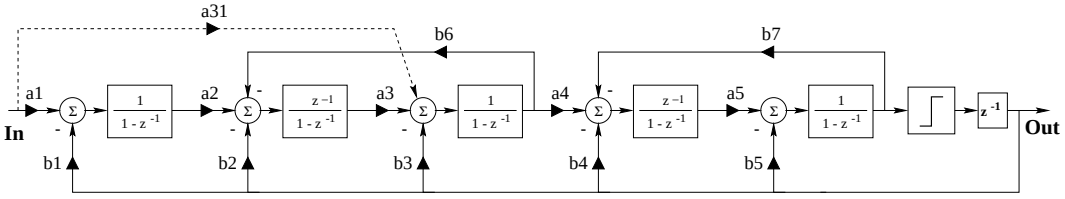

Figure 10: Block diagram of IFLF5 modulator complemented by two finite NTF zero feedbacks (b_6 and b_7) and an additional STF zero feed-forward path (a_{31}).

The design procedure for the NTF is similar to the design of a regular highpass filter. One notable distinction is that the focal point of the design is the filter stopband rather than the passband. As a matter of fact, there hardly exist any specifications for the NTF passband (i.e., the signal stopband) other than limiting the high-frequency noise gain to avoid a modulator overload. This leaves few restrictions for the pole placement procedure.

Figure 11 shows the frequency characteristics of an STF-NTF pair customized to the given specifications using the DelSi simulator. This particular numerical solution has been derived under the additional constraint of keeping the swings of the five integrator outputs balanced while assuming equal feed-forward and the feed-back coefficient in each stage to simplify the physical implementation. The resulting set of filter coefficients is shown below.

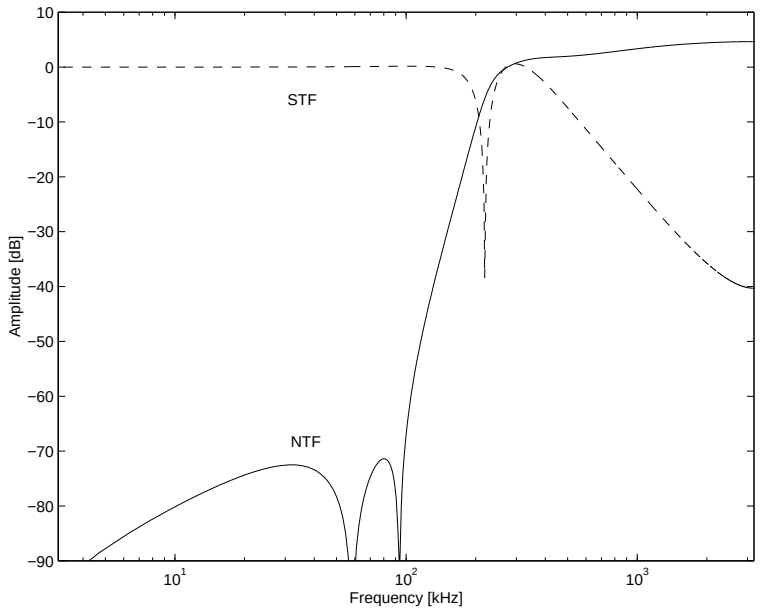

Figure 11: Numerically optimized STF and NTF of the ILFL5 modulator ($f_s = 6.4$ MHz).

$$\begin{aligned} a_1 = b_1 &= 0.166667 & a_4 = b_4 &= 0.300000 \\ a_2 = b_2 &= 0.125000 & a_5 = b_5 &= 0.500000 \\ a_3 = b_3 &= 0.333333 & b_6 &= 0.009357 \\ a_{31} &= 0.152500 & b_7 &= 0.016304 \end{aligned}$$

Note that apart from the zero placing coefficients a_{31}, b_6 and b_7, all values represent simple integer fractions. Since the coefficients will be realized by element area ratios (e.g. of capacitors), this simplifies the layout.

As mentioned before, high-order single-bit converters are only conditionally stable. The above solution is no exception. In fact, the presented 5^{th} order modulator is likely to saturate or fall into a cyclic behavior, i.e., become unstable, if its input signal exceeds a critical value of approximately 60% of the analog feedback signal for any extended amount of time (e.g. several dozen clock cycles). To avoid such an overload condition, the input signal must be limited in amplitude. In addition, practical modulators are equipped with an overload detection circuit, which resets the entire system as soon as an unstable mode of operation is detected.

Figure 12 shows the output spectrum of the given IFLF5 modulator in presence of a 8 kHz sinusoidal input signal of -9 dB relative power. The displayed spectrum, a DelSi simulation, has been computed by averaging the results of eight 2^{17} point FFT's. The

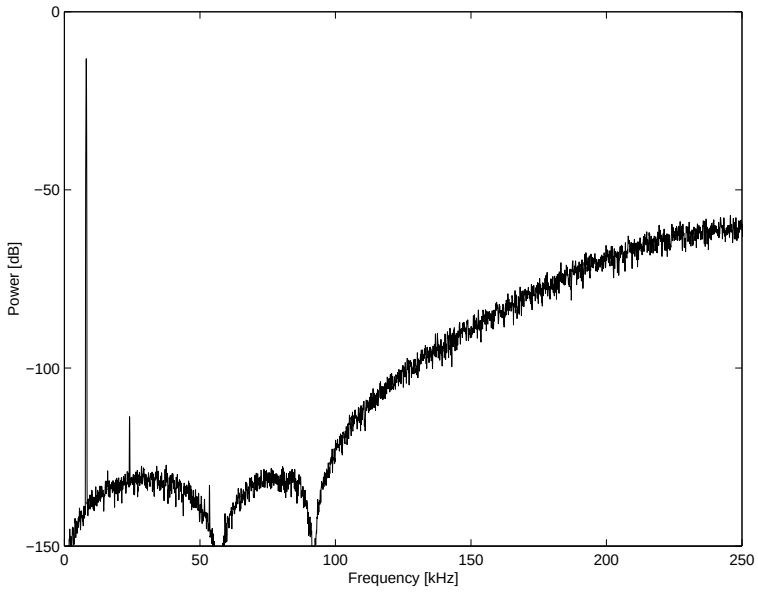

Figure 12: Spectral response of ILFL5 modulator in presence of a 8 kHz sinusoidal input signal (DelSi simulation with f_s=6.4 MHz).

displayed example yields an SNR of 91 dB. This corresponds to a resolution of 15 bits. The plot also reveals a characteristic 3^{rd} harmonic located approximately 100 dB below the input signal. Such a low harmonic power is deemed harmless. We thus conclude that the presented solution conforms well to the given modulator specifications.

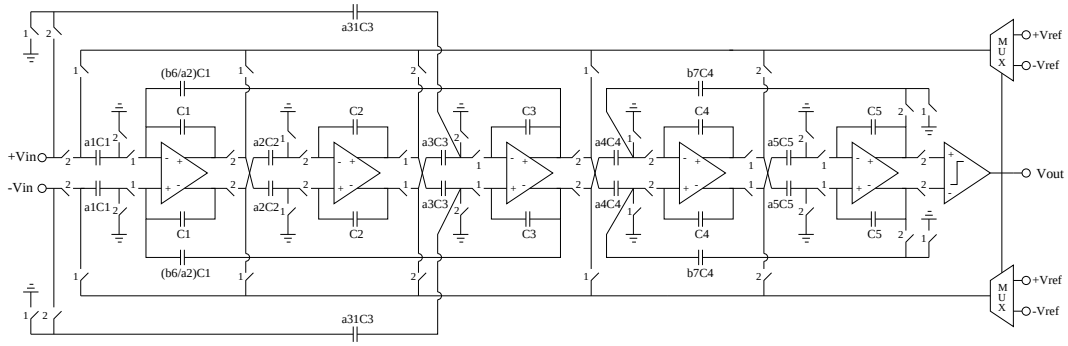

Figure 13: Fully-Differential SC implementation of IFLF5 modulator.

The last step in the design procedure is the actual physical implementation. The most common monolithic solution for an extended audio range application is an SC circuit. Figure 13 depicts the schematic of a fully-differential SC implementation of the

presented IFLF5 modulator. The presented circuit employs a standard 2-phase non-overlapping clocking scheme. Furthermore, it exploits the symmetry between the feed-forward and feed-back coefficients of each integrator stage by realizing both coefficients by time-multiplexing a single capacitor. Another special feature of this circuit is the modified feedback path b_6/a_2. By eliminating the switches in the corresponding feedback path, this zero loop could be extended over three amplifier stages. This not only saved two switch pairs but also reduced the coefficient spread.

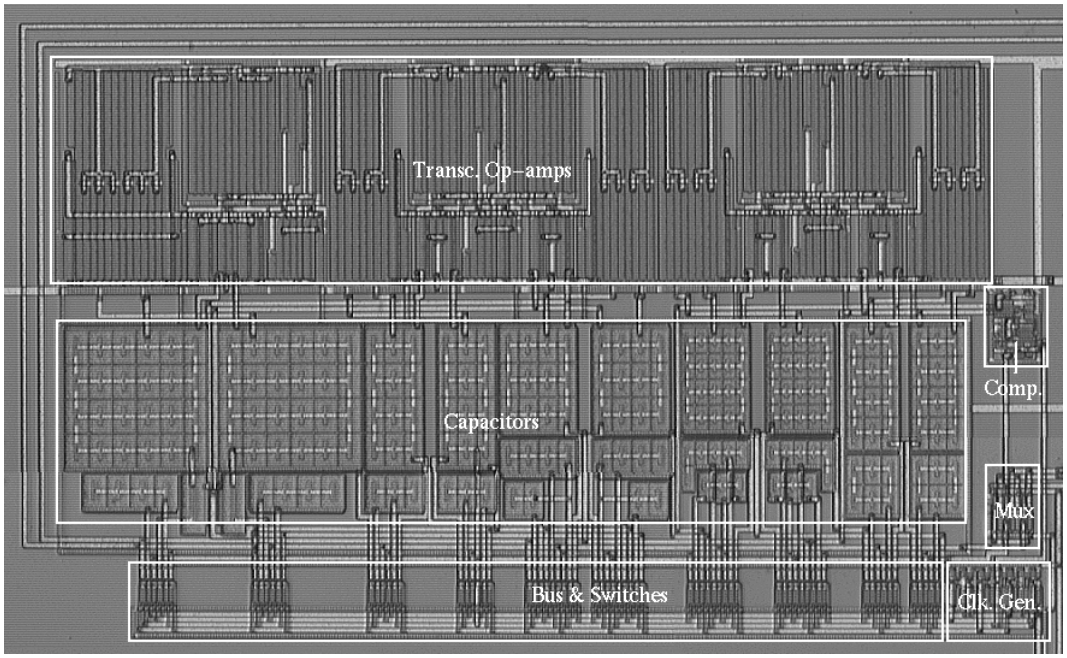

Figure 14: Micro-photograph of complete IFLF5 modulator in $1.2\mu m$ double-poly CMOS technology (Size: $820\mu m \times 470\mu m$).

Figure 14 shows a micro-photograph of the modulator circuit. An important objective of this layout has been to maximize the physical distance between analog and digital sub-units to minimize crosstalk. The top row shows the five fully-differential CMOS amplifiers required to emulate the discrete-time integrators. They have been realized by folded-cascode transconductance gain stages [20] and exhibit a bandwidth of approximately 50 MHz. The middle section of the layout accommodates the linear double-poly capacitors forming the filter coefficients. One can easily discern the pairwise identical unit-element arrays representing the complementary capacitors of the two signal paths. The bottom portion of the picture, finally, shows the digital section. It consists of the

switches (realized by CMOS transmission gates), the adjacent clock bus below and the necessary non-overlapping clock generator (bottom right). The comparator and the two multiplexers are realized by the two small cells on the lower right periphery in figure 14.

The depicted circuit occupies a chip area of less than 0.4 mm^2 and, when operated from a single 5 V supply, dissipates approximately 25 mW of power.

Figure 15 shows a measured spectrum of the IFLF5 modulator obtained with an 8 kHz sinusoidal input signal and a sampling rate of 6.4 MHz. To minimize the variance of the output noise, we have averaged 200 FFT's computed from 2^{17} time samples each. The resulting plot confirms the high dynamic range of the system. The two NTF zeros, while partially submerged in white noise, are still visible. The recorded white noise stems predominantly from the first integrator stage, in particular the kT/C contribution of the two input capacitors.

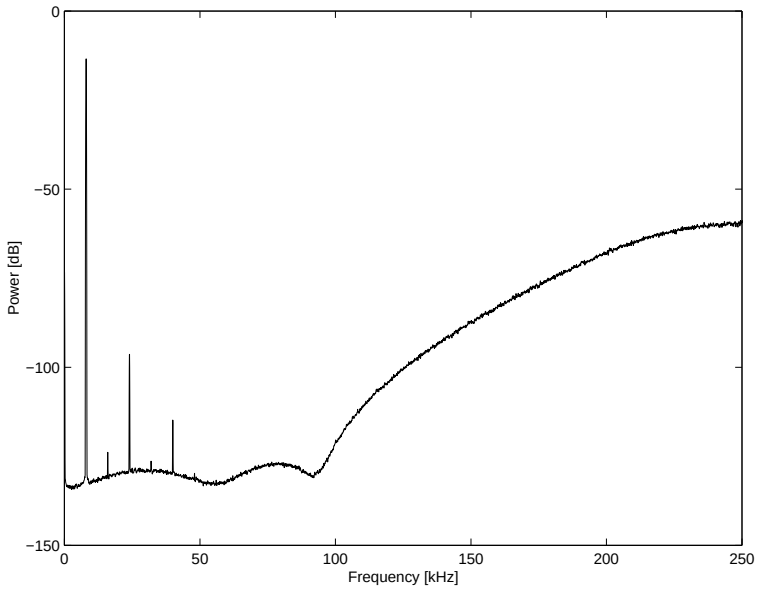

Figure 15: Measured spectrum of IFLF5 modulator obtained with a sinusoidal input signal of 8 kHz and a sampling rate of 6.4 MHz.

To complete the entire ADC system, the modulator circuit in figure 14 has to be embedded between a continuous-time pre-filter (to avoid aliasing) and a digital low-pass/decimator circuit (to lower the sampling rate to the Nyquist frequency and convert the 1-bit modulator output to a standard 16 bit format). Both of these cells can be realized by a standard CMOS process. However, a detailed discussion of their implementation would exceed the scope of this article and will therefore not be attempted here.

In conclusion, we would like to repeat that the quintessential element of a $\Delta\Sigma$ based ADC is the analog modulator loop. It represents the most sensitive system component and thus bears most of the burden of satisfying the converter specifications.

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