

## sys-box & sys-card Connector Descriptions

April 25, 2000

<u>ID</u>	<u>Type</u>	<u>No. of pins</u>	<u>Description</u>
P1, P2	VHDCI	68	"SCSI" ICED bus to host - on d-card-s
P3, P4	High-dens.	70	d-card-s to sys-card
P11-P16	DIP	16	internal IBUS to protoboard/P21-P24
P21-P25	DIP	16	SIMM (memory) connections from protoboard/P11-P14
P31-P36	Logic An.	20	internal IBUS taps to Logic Analyzer (LA)
P41A, P42A	Logic An.	20	multiplexed internal IBUS (DB/{CB,AB}) to LA
P42B, P42B	Logic An.	20	pin-for-pin copy of P4xA
P53, P55	Logic An.	20	SIMM taps (w/out data lines) to LA
P61	Logic An.	20	network xface taps to LA
P71	DIP	16	network xface connections from protoboard
P81	DIP	16	LCD (U61) connections from protoboard; & some address bits
P91	SIMM	72	SIMM socket - currently for 8 MB memory, 16 MB possible
P101	banana	1	Ground - black
P102	banana	1	+5 V. - red
P103	banana	1	+12 V. - green
P104	banana	1	-5 V. - yellow
P105	banana	1	-12 V. - white
P110	BNC	2	ICEDnet connection

### Notes:

- 1) P1 and P2 are unstacked
- 2) typically P11-P14 can be directly connected to P21-P24 (resp.) with ribbon cable
  - if data &/or address lines are needed on the protoboard, some or all of these must go to the protoboard
- 3) address bits A0, A1, A21, A22 & A23 are also available on P81
- 4) P1x and P2x rows are separated by 0.3" pin-to-pin
- 5) P4{1,2}A and P4{1,2}B provided for simultaneous timing and state analysis on our HP 166x logic analyzers; A for timing, say, and B for state.