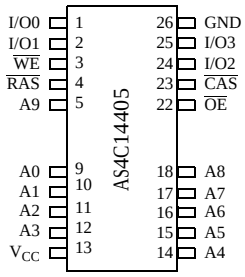
5V 1M×4 CMOS DRAM (EDO)

Features

- Organization: 1,048,576 words × 4 bits
- High speed
  - 60 ns $\overline{RAS}$ access time
  - 25 ns hyper page cycle time
  - 17 ns $\overline{CAS}$ access time
- Low power consumption
  - Active: 385 mW max
  - Standby: 5.5 mW max, CMOS I/O
- Extended data out
- 1024 refresh cycles, 16 ms refresh interval
  - $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Read-modify-write
- TTL-compatible, three-state I/O
- JEDEC standard package and pinout
  - 300 mil, 26/20-pin SOJ
- 5V power supply

Pin arrangement

SOJ



Pin designation

Pin(s)	Description
A0 to A9	Address inputs
$\overline{RAS}$	Row address strobe
I/O0 to I/O3	Input/output
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{CAS}$	Column address strobe
V_{CC}	Power
GND	Ground

DRAM

Selection guide

	Symbol	AS4C14405-60	Unit
Maximum $\overline{RAS}$ access time	t_{RAC}	60	ns
Maximum column address access time	t_{AA}	30	ns
Maximum $\overline{CAS}$ access time	t_{CAC}	17	ns
Maximum output enable ($\overline{OE}$) access time	t_{OEA}	15	ns
Minimum read or write cycle time	t_{RC}	110	ns
Minimum hyper page mode cycle time	t_{HPC}	25	ns
Maximum operating current	I_{CC1}	70	mA
Maximum CMOS standby current	I_{CC5}	1.0	mA

Functional description

The AS4C14405 is a high performance CMOS Dynamic Random Access Memory organized as 1,048,576 words × 4 bits. The AS4C14405 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in a high speed component required by high performance systems.

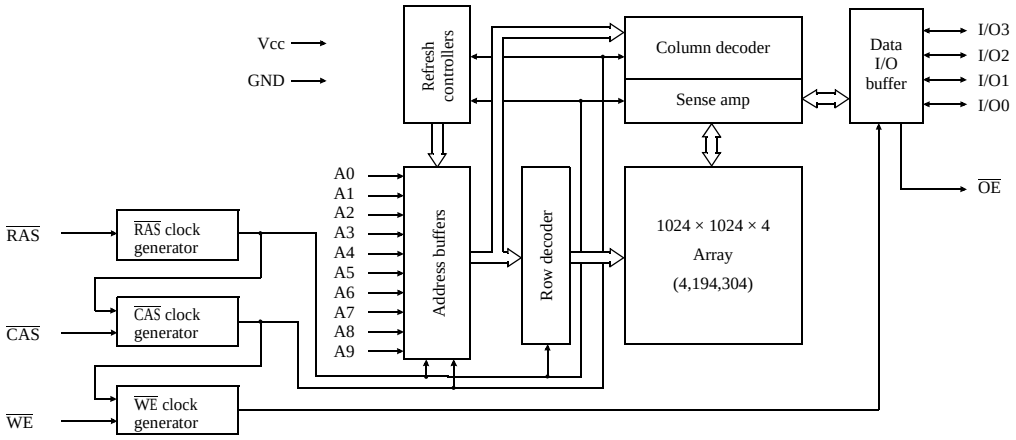
The AS4C14405 features a high speed page mode operation in which high speed read, write and read-write are performed on any of the 1024 × 4 bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Very fast $\overline{CAS}$ to output access time eases system design. In contrast to 'fast page mode' devices, data remains active on outputs after $\overline{CAS}$ is de-asserted high, giving system logic more time to latch the data.

Refresh on the 1024 address combinations of A0 to A9 during a 16 ms period is accomplished by performing any of the following:

- $\overline{RAS}$-only refresh cycles
- Hidden refresh cycles
- $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles
- Normal read or write cycles

The AS4C14405 is available in JEDEC standard 20/26-pin plastic SOJ packages. System level features include single power supply of 5.0 ± 0.5V tolerance and direct interface with TTL logic families.

Logic block diagram



Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage	AS4C14405	V_{CC}	4.5	5.0	5.5	V
		GND	0.0	0.0	0.0	V
Input voltage	AS4C14405	V_{IH}	2.4	–	V_{CC}	V
		V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature		T_A	0		70	°C

†V_{IL} min -3.0V for pulse widths less than 5 ns.

Recommended operating conditions apply throughout this document unlesss otherwise specified.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{in}	-1.0	+7.0	V
Input voltage (I/Os)	$V_{I/O}$	-1.0	V_{CC} + 0.5	V
Power supply voltage	V_{CC}	-1.0	+7.0	V
Storage temperature (plastic)	T_{STG}	-55	+150	°C
Soldering temperature × time	T_{SOLDER}	–	260 × 10	°C × sec
Power dissipation	P_D	–	1	W
Short circuit output current	I_{out}	–	50	mA

DC electrical characteristics

			-60			
Parameter	Symbol	Test conditions	Min	Max	Unit	Notes
Input leakage current	I_{IL}	0V ≤ V_{in} ≤ +5.5V, Pins not under test = 0V	-2	+2	µA	
Output leakage current	I_{OL}	D_{OUT} disabled, 0V ≤ V_{out} ≤ +5.5V	-10	+10	µA	
Operating power supply current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, Address cycling; t_{RC}=min	–	70	mA	1,2
TTL standby power supply current	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	–	2.0	mA	
Average power supply current, $\overline{RAS}$ refresh mode or CBR	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ V_{IH}, t_{RC} = min of $\overline{RAS}$ low after $\overline{CAS}$ low	–	70	mA	1
Hyper page mode average power supply current	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{HPC} = min	–	90	mA	1, 2
CMOS standby power supply current	I_{CC5}	$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V	–	1.0	mA	
Output voltage	V_{OH}	I_{OUT} = -5.0 mA	2.4	–	V	
	V_{OL}	I_{OUT} = 4.2 mA	–	0.4	V	
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	70	mA	

DRAM

AC parameters common to all waveforms

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Symbol	Parameter	Min	Max	Unit	Notes
t_{RC}	Random read or write cycle time	110	–	ns	
t_{RP}	$\overline{RAS}$ precharge time	40	–	ns	
t_{RAS}	$\overline{RAS}$ pulse width	60	10K	ns	
t_{CAS}	$\overline{CAS}$ pulse width	13	10K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	45	ns	6
t_{RAD}	$\overline{RAS}$ to column address delay time	15	30	ns	7
t_{RSH}	$\overline{CAS}$ to $\overline{RAS}$ hold time	15	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CAS}$ hold time	60	–	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	ns	
t_{ASR}	Row address setup time	0	–	ns	
t_{RAH}	Row address hold time	10	–	ns	
t_T	Transition time (rise and fall)	2	50	ns	4,5
t_{REF}	Refresh period	–	16	ms	3
t_{CP}	CAS precharge time	10	–	ns	
t_{RAL}	Column address to $\overline{RAS}$ lead time	30	–	ns	
t_{ASC}	Column address setup time	0	–	ns	
t_{CAH}	Column address hold time	10	–	ns	

DRAM

Read cycle

		-60			
Symbol	Parameter	Min	Max	Unit	Notes
t_{RAC}	Access time from $\overline{RAS}$	–	60	ns	6
t_{CAC}	Access time from $\overline{CAS}$	–	17	ns	6,13
t_{AA}	Access time from address	–	30	ns	7,13
t_{RCS}	Read command setup time	0	–	ns	
t_{RCH}	Read command hold time to $\overline{CAS}$	0	–	ns	9
t_{RRH}	Read command hold time to $\overline{RAS}$	0	–	ns	9

Write cycle

Symbol	Parameter	-60 Min	-60 Max	Unit	Notes
t_{WCS}	Write command setup time	0	–	ns	11
t_{WCH}	Write command hold time	10	–	ns	11
t_{WP}	Write command pulse width	10	–	ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	15	–	ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	15	–	ns	
t_{DS}	Data-in setup time	0	–	ns	12
t_{DH}	Data-in hold time	10	–	ns	12

Read-modify-write cycle

Symbol	Parameter	-60 Min	-60 Max	Unit	Notes
t_{RWC}	Read-write cycle time	135	–	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay time	77	–	ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay time	35	–	ns	11
t_{AWD}	Column address to $\overline{WE}$ delay time	47	–	ns	11

Refresh cycle

Symbol	Parameter	-60 Min	-60 Max	Unit	Notes
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$)	10	–	ns	3
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$)	10	–	ns	3
t_{RPC}	$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	0	–	ns	
t_{CPT}	$\overline{CAS}$ precharge time (CBR counter test)	10	–	ns	

Hyper page mode cycle

		-60			
Symbol	Parameter	Min	Max	Unit	Notes
t_{CPWD}	$\overline{CAS}$ precharge to $\overline{WE}$ delay time	52	–	ns	
t_{CPA}	Access time from $\overline{CAS}$ precharge	–	35	ns	13
t_{RASP}	$\overline{RAS}$ pulse width	60	100K	ns	
t_{DOH}	Previous data hold time from $\overline{CAS}$	5	–	ns	
t_{REZ}	Output buffer turn off delay from $\overline{RAS}$	0	15	ns	
t_{WEZ}	Output buffer turn off delay from $\overline{WE}$	0	15	ns	
t_{OEZ}	Output buffer turn off delay from $\overline{OE}$	0	15	ns	
t_{HPC}	Hyper page mode cycle time	25	–	ns	
t_{HPRWC}	Hyper page mode RMW cycle	60	–	ns	
t_{RHCP}	$\overline{RAS}$ hold time from $\overline{CAS}$	35	–	ns	

Output enable

		-60			
Symbol	Parameter	Min	Max	Unit	Notes
t_{CLZ}	$\overline{CAS}$ to output in Low Z	0	–	ns	8
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ access time	–	15	ns	
t_{OED}	$\overline{OE}$ to data delay	15	–	ns	
t_{OEZ}	Output buffer turnoff delay from $\overline{OE}$	0	15	ns	8
t_{OEH}	$\overline{OE}$ command hold time	10	–	ns	
t_{OLZ}	$\overline{OE}$ to output in Low Z	0	–	ns	
t_{OFF}	Output buffer turn-off time	0	15	ns	8,10

Notes

1 I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on frequency.

2 I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

3 An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).

4 AC Characteristics assume t_T = 2 ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF, V_{IL} (min) ≥ GND and V_{IH} (max) ≤ V_{CC}.

5 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

6 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

7 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

8 Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).

9 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10 t_{OFF} (max) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels. t_{OFF} is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

11 t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If t_{WS} ≥ t_{WS} (min) and t_{WH} ≥ t_{WH} (min), the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If t_{RWD} ≥ t_{RWD} (min), t_{CWD} ≥ t_{CWD} (min) and t_{AWD} ≥ t_{AWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.

12 These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-write cycles.

13 Access time is determined by the longest of t_{CAA} or t_{CAC} or t_{CPA}

14 t_{ASC} ≥ t_{CP} to achieve t_{PC} (min) and t_{CPA} (max) values.

15 These parameters are sampled and not 100% tested.

16 These characteristics apply to AS4C14405 5V devices.

AC test conditions

- Access times are measured with output reference levels of V_{OH} = 2.4V and V_{OL} = 0.4V, V_{IH} = 2.4V and V_{IL} = 0.8V
- Input rise and fall times: 2 ns

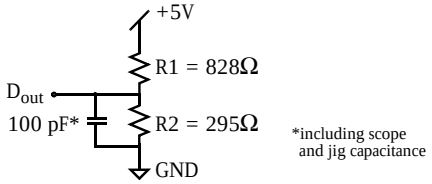
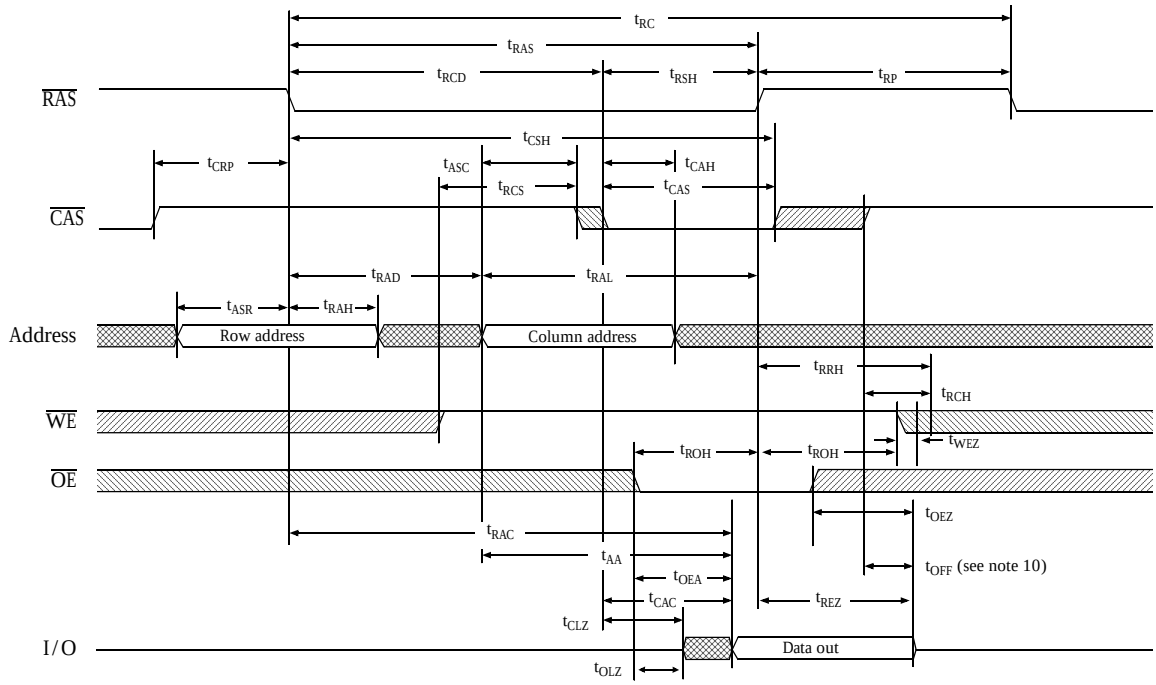


Figure A: Equivalent output load

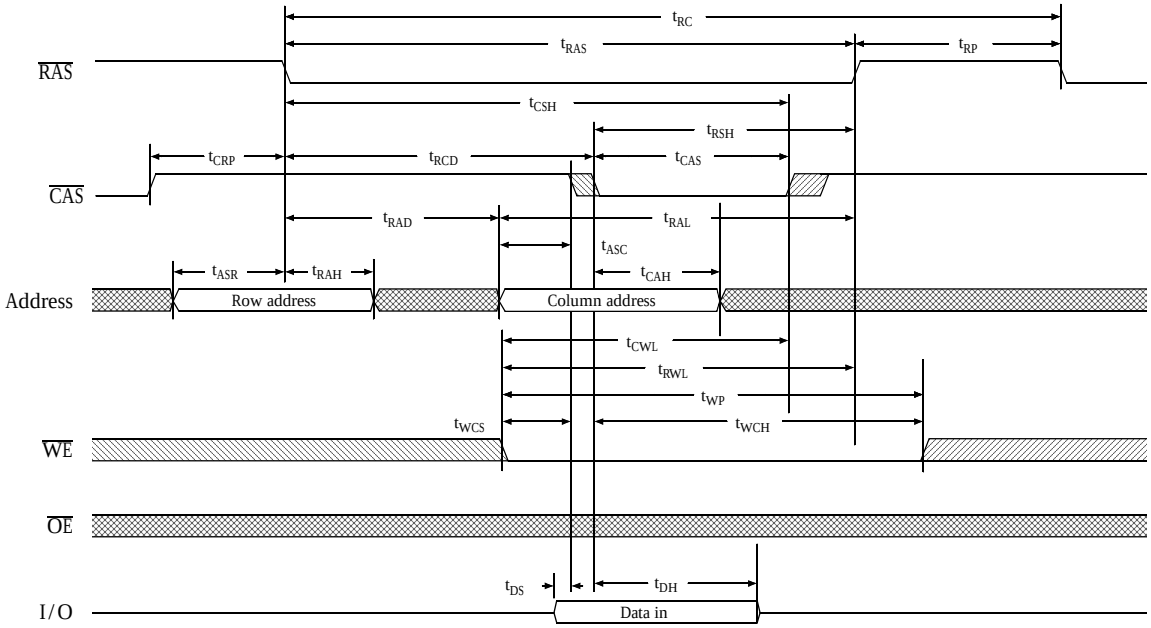
Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform

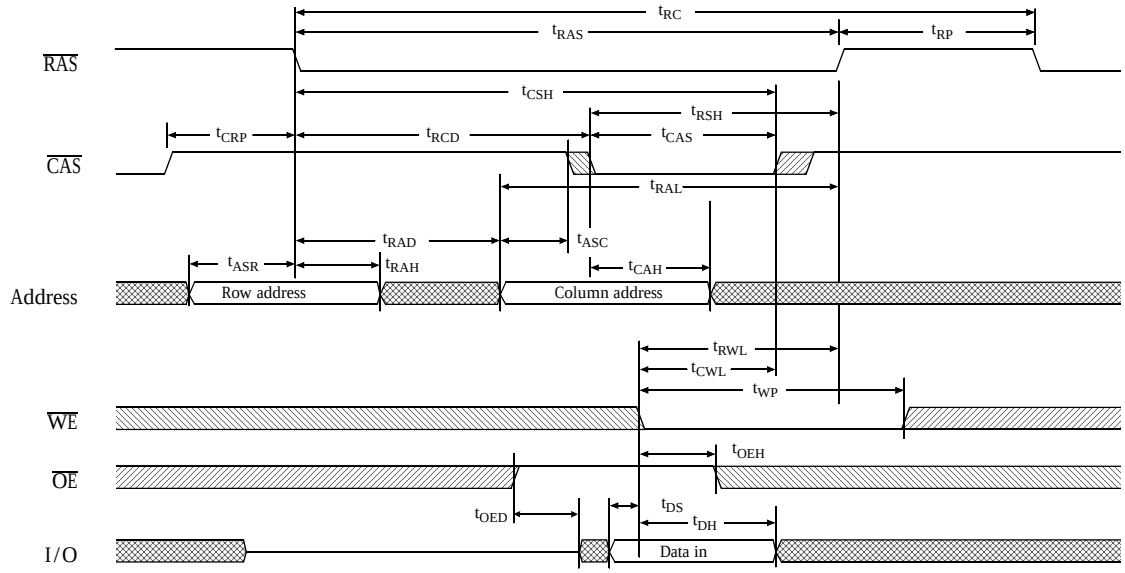


Early write waveform

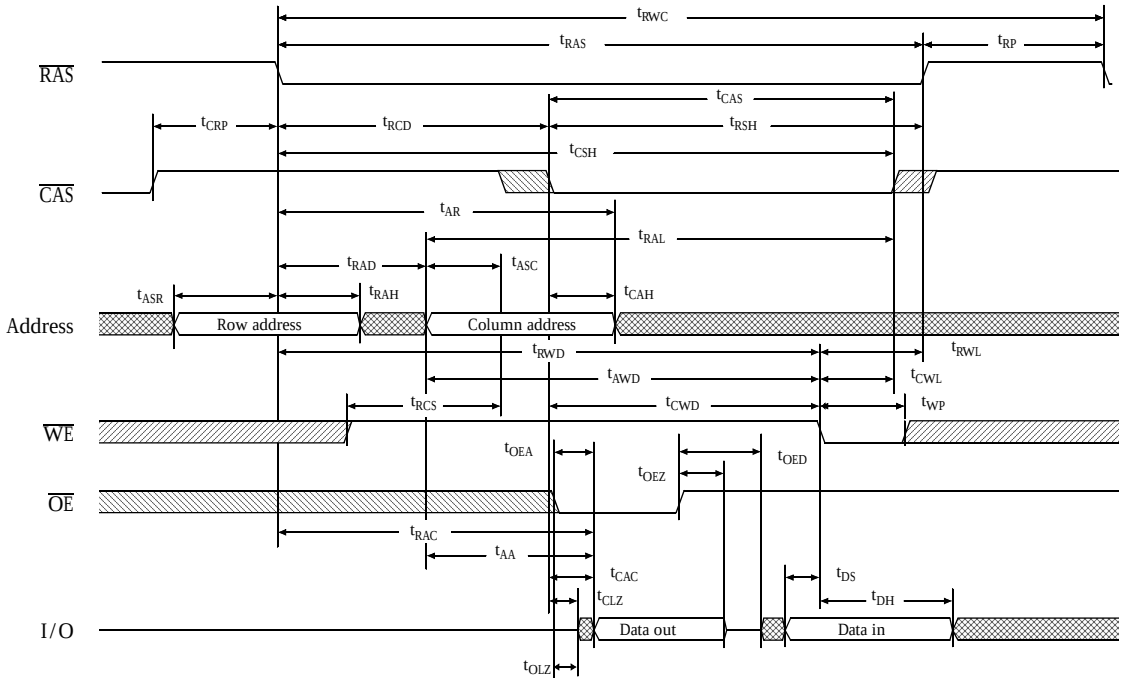


Write waveform

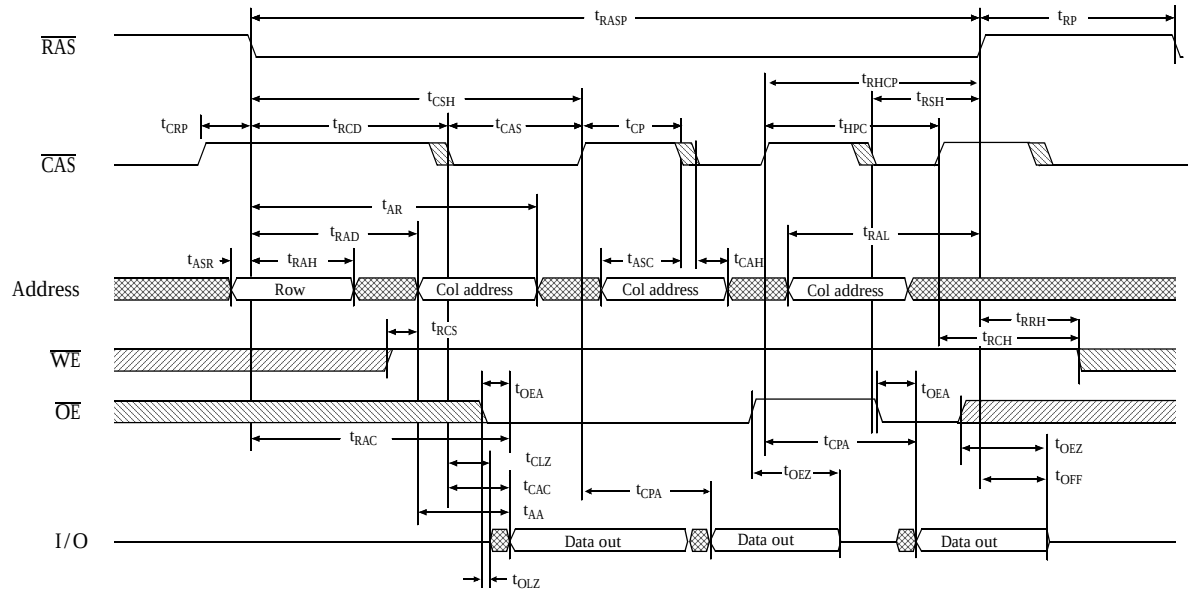
$\overline{OE}$ controlled



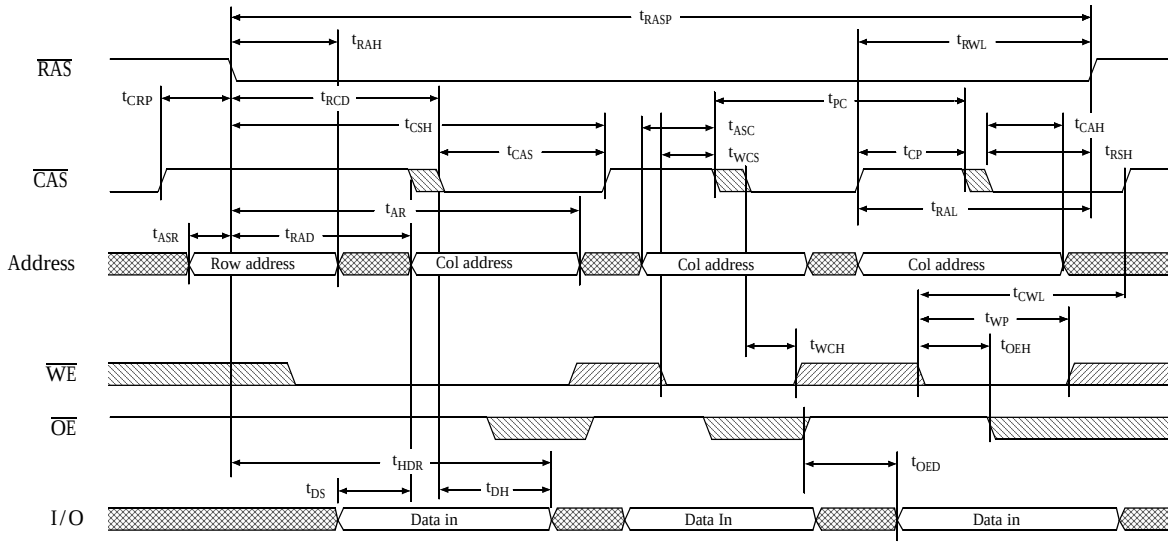
Read-modify-write waveform



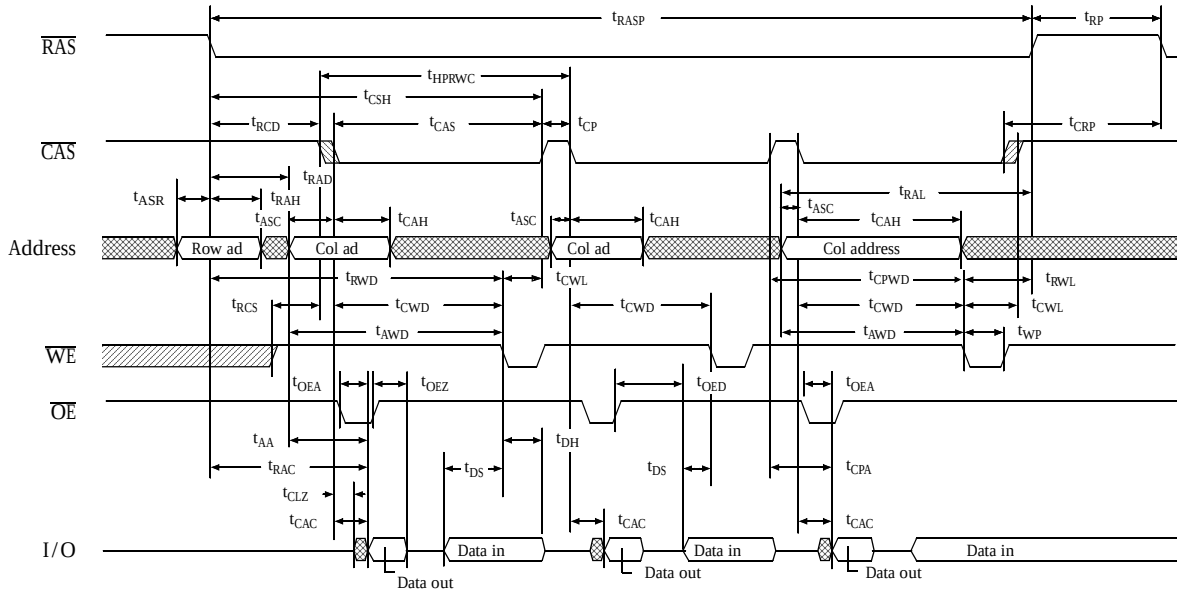
Hyper page mode read waveform



Hyper page mode early write waveform



Hyper page mode read-modify-write waveform



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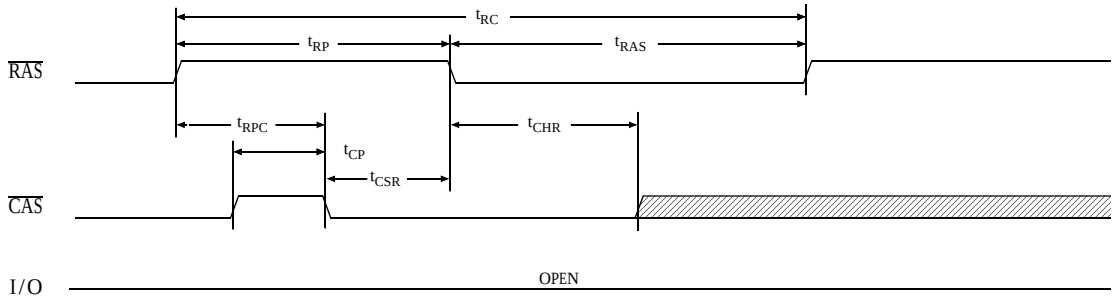
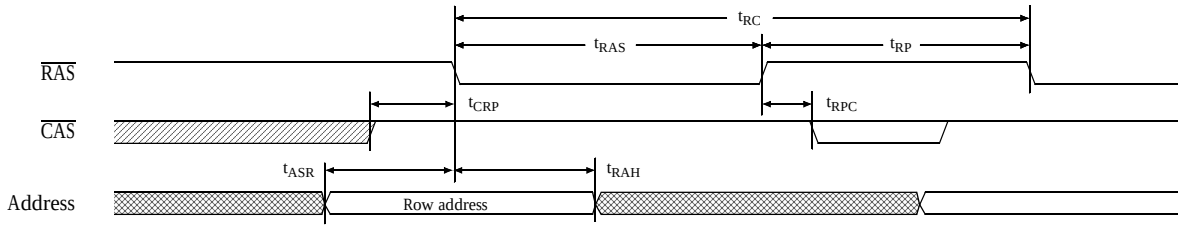
$\overline{CAS}$ before $\overline{RAS}$ refresh waveform

$\overline{WE}$ = A = V_{IH} or V_{IL}

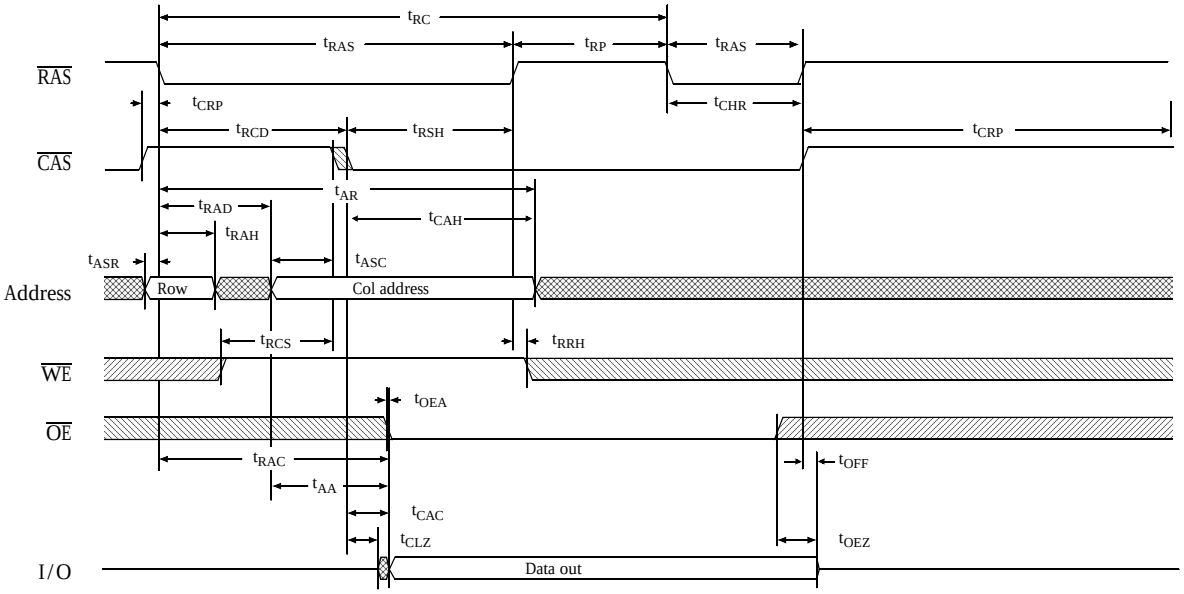


$\overline{RAS}$ only refresh waveform

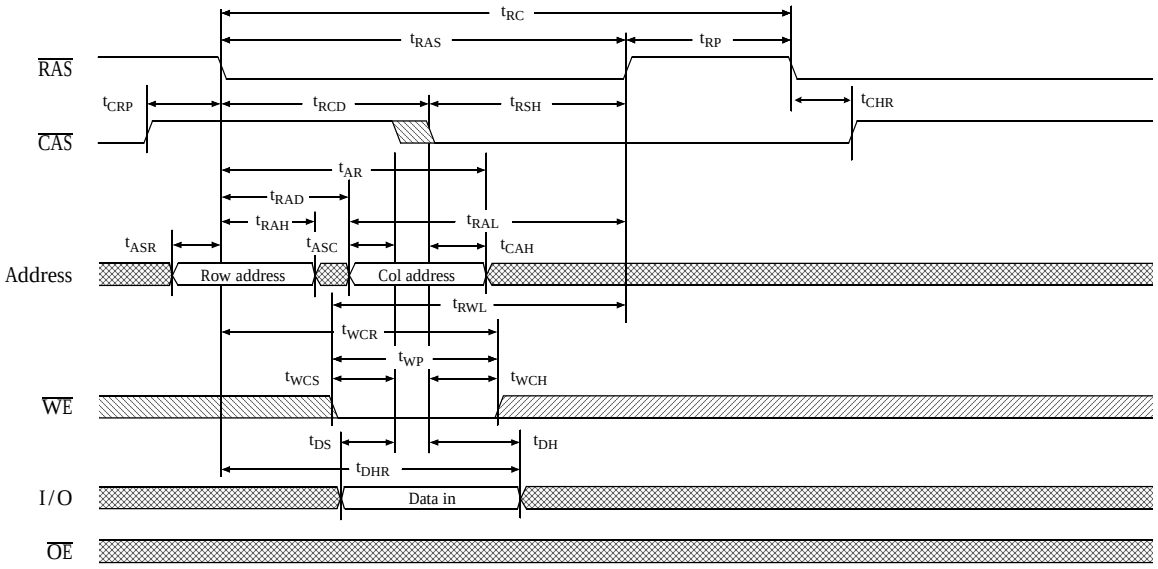
$\overline{WE}$ = $\overline{OE}$ = V_{IH} or V_{IL}



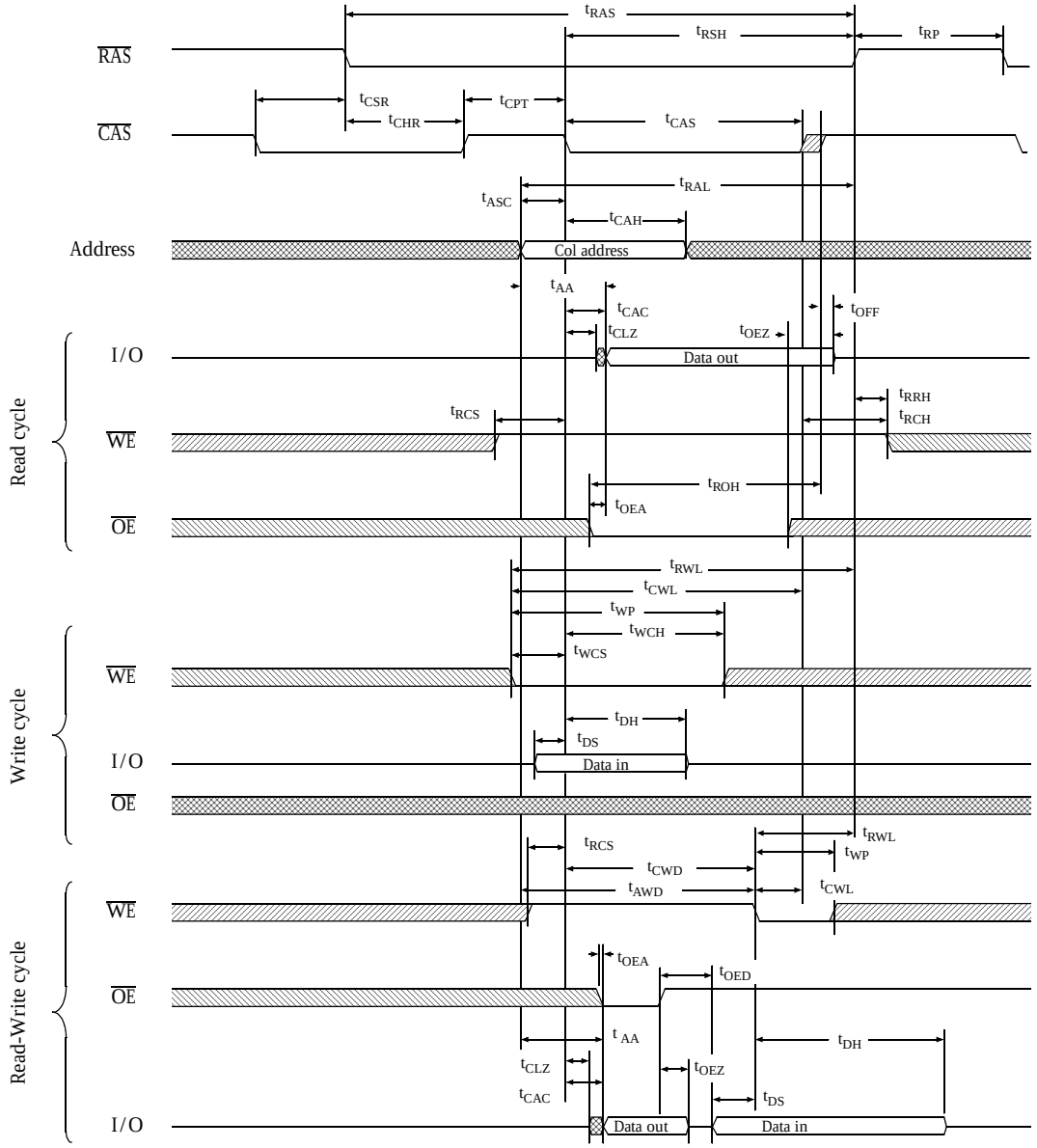
Hidden refresh waveform (read)



Hidden refresh waveform (write)



CAS before RAS refresh counter test waveform



Capacitance [15]

f = 1 MHz, T_a = Room temperature

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN1}	A0 to A9	V_{in} = 0V	5	pF
	C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	7	pF
I/O capacitance	$C_{I/O}$	I/O0 to I/O3	V_{in} = V_{out} = 0V	7	pF

AS4C14405 ordering information

Package \ $\overline{RAS}$ access time		60 ns
Plastic SOJ, 300 mil, 26/20-pin	5V	AS4C14405-60JC

AS4C14405 part numbering system

AS4	C	14405	–XX	X	C
DRAM prefix	C = 5V CMOS	Device number	$\overline{RAS}$ access time	Package: J = 26/20-pin SOJ 300 mil	Commercial temperature range, 0°C to 70 °C

DRAM