ICED Protosys Hardware System Tests

May 27, 2000

Connect P15, P16 to protoboard, connect as shown on right:

Pin Settings: 0 = 0 Volts, 1 = +5 Volts

Test No.	Test Type	Test/ Other Connections	Monitor Program/ cmd.	End of IBUS	P16-(1-4) DB:CE	P16-(13-16) DB:D/-R	P16-(5-7) AB:CE	P16-(10-12) AB:D/-R	P16-8 CB:CE	P15-(9,10,13-16) CB(7,6,3-0):D/-R	P15-(11,12) CB(5,4):D/-R
1	static	Marching 1's, 0's; thru all IBUS	`icedtest123`	host (Sun, FPGA)	1	1	1	1	1	1	1
			`c ; 9`	sys-card	1	0	1	0	1	0	0
		no other connections than P15, P16			P16-(1-4)	P16-(13-16)	P16-(5-7)	P16-(10-12)	P16-8	P15-(9,10,13-16)	P15-(11,12)
2	static	1 w/Feedback, DBUS driving CABUS	`icedtest123`	host (Sun, FPGA)	1	1	1	0	1	0	0
			`c ; 2`	sys-card	1	0	1	1	1	1	1
		P11 to P13, P12 to P14			P16-(1-4)	P16-(13-16)	P16-(5-7)	P16-(10-12)	P16-8	P15-(9,10,13-16)	P15-(11,12)
3	static	1 w/Feedback, CABUS driving DBUS	`icedtest123`	host (Sun, FPGA)	1	0	1	1	1	1	1
			`c ; 3`	sys-card	1	1	1	0	1	0	0
		P11 to P13, P12 to P14			P16-(1-4)	P16-(13-16)	P16-(5-7)	P16-(10-12)	P16-8	P15-(9,10,13-16)	P15-(11,12)
4	dynamic	Memory test - no CPU	`icedtest4`	host (Sun, FPGA)	1	CWR	1	1	1	1	0
		8 MB SIMM in sys-card socket	`c ; m`	sys-card	1	-CWR	1	0	1	0	1
					P16-(1-4)	P16-(13-16)	P16-(5-7)	P16-(10-12)	P16-8	P15-(9,10,13-16)	P15-(11,12)
		P11 to P21, P12 to P22, P13 to P23, P14 to P24 P25 to protoboard (SIMM drive) P81 to protoboard (AB[0,1,21-23])									
5	dynamic	same as 4, but memory and LCD driven by ICED canned CPU	`icedtest5` ICED prog: `lcdp.hex` `i ; c ; i ; l [lcdp.hex] ; p [CRs] ; e`								

NOTES:
- "CE" is the chip enable for an IBUS transceiver.
- "D/-R" sets the individual direction of a signal through an IBUS transceiver.
- For DBUS and ABUS each byte's D/-R lines are connected together.
- For CBUS the D/-R lines remain separate.

NOTES:

1. "static" tests: about 1 second between changes in LEDs
2. "dynamic" tests: IBUS clock (CCLK1) run at 1 MHz (EVC1 POM clock at 8 MHZ)
3. For all of these tests, the system is fully connected and the specified version of the monitor program is running on the host.
4. We currently do not have an ICEDnet interface designed or wired up; use the test specified in the document of NOTE 6 below.
5. The "host (Sun, FPGA)" P15 and P16 connections are automatically made for you by the Monitor Program.
6. This document should be used in conjunction with the testing guide: http://www.ele.uri.edu/iced/protosys/hardware/testing/Protosys-testing.pdf
7. The monitor program shell scripts are in: /usr/local/cadbin on leviathan; this is normally in everyone's path.

Test Specific Notes:

1. a. This test does not need any DIP cable jumpers on the sys-card.
   b. There is no feedback to the host, so user must visually verify that the LEDs are doing the right things.
   c. Only one of the 64 IBUS LEDs will have a different value from the others during the subtests.

2. a. This test requires the specified DIP cable jumpers on the sys-card.
   b. There is feedback to the host; the monitor program reports success or failure.
   c. It is also helpful to visually verify the LEDs' lighting sequence.
   d. A working system's LEDs will always show DBUS={CBUS,ABUS}; that is, the top row of LEDs will look the same as the bottom row.

3. a. - d. Same as for Test 2.

4. a. This test requires the specified DIP cable jumpers on the sys-card.
   b. There is feedback to the host; the monitor program reports success or failure.
   c. The EVC1 clock (POM) frequency should be set to 8 MHz for an IBUS frequency of 1 MHz. Use monitor command: `f`
   d. This test requires memory interface logic on the protoboard. A pre-wired protoard with this logic is available; see Gus Uht.
   e. This test uses the host controller of the ICED canned computer, but not the CPU itself.

5. a. This test requires the specified DIP cable jumpers on the sys-card.
   b. There is NO feedback to the host; the user must verify that the correct message appears on the sys-card's LCD display.
      First: on the top line, the message: "ICED sys-card #1" shifts in from the right.
      Second: on the bottom line, the message: "URI Jan. 2, 2000" is written a character at a time from left to right, no shifting.
   c. The EVC1 clock (POM) frequency should be set to 8 MHz for an IBUS frequency of 1 MHz. Use monitor command: `f`
   d. This test requires both memoryand LCD interface logic on the protoboard. A pre-wired protoard with this logic is available; see Gus Uht.
   e. This test uses a version of the complete ICED canned computer.