

Interactive High-Performance Processor Understanding Via the Web



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Motivation

- CPU chip *complexity* high and growing
 - 10's of millions of transistors → billions
- → *functional verification* costs growing
- → *time-to-market* excessive
- → *education* difficult
- → *debugging* difficult

Related Work

- Many specialized simulators, e.g., IBM BRAT
 - Not readily adaptable to other machines
- “General Purpose” visualizers, e.g., Stanford Rivet
 - May be adaptable to many types of systems
 - Scalability is an issue: much state
 - Often, adaptability is through custom scripts
 - LevoVis based on std. XML and SVG
 - Not readily accessible; LevoVis is Web-based

CPU Performance Basics

- Two elements to processor performance - P :
 - Clock frequency – f
 - Technology dependent
 - Instructions executed per cycle – IPC
 - Architecture and Implementation dependent
- Fundamental relation:

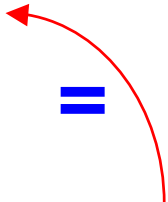
$$P = f * IPC$$

- **LEVO** focuses on high IPC via ILP →

Instruction Level Parallelism (ILP)

- Execute more than 1 instruction per cycle
- Example:

1. $A = B + C$
2. $D = E + F$
3. $G = A + H$



instructions **1** and **2** can execute in parallel;

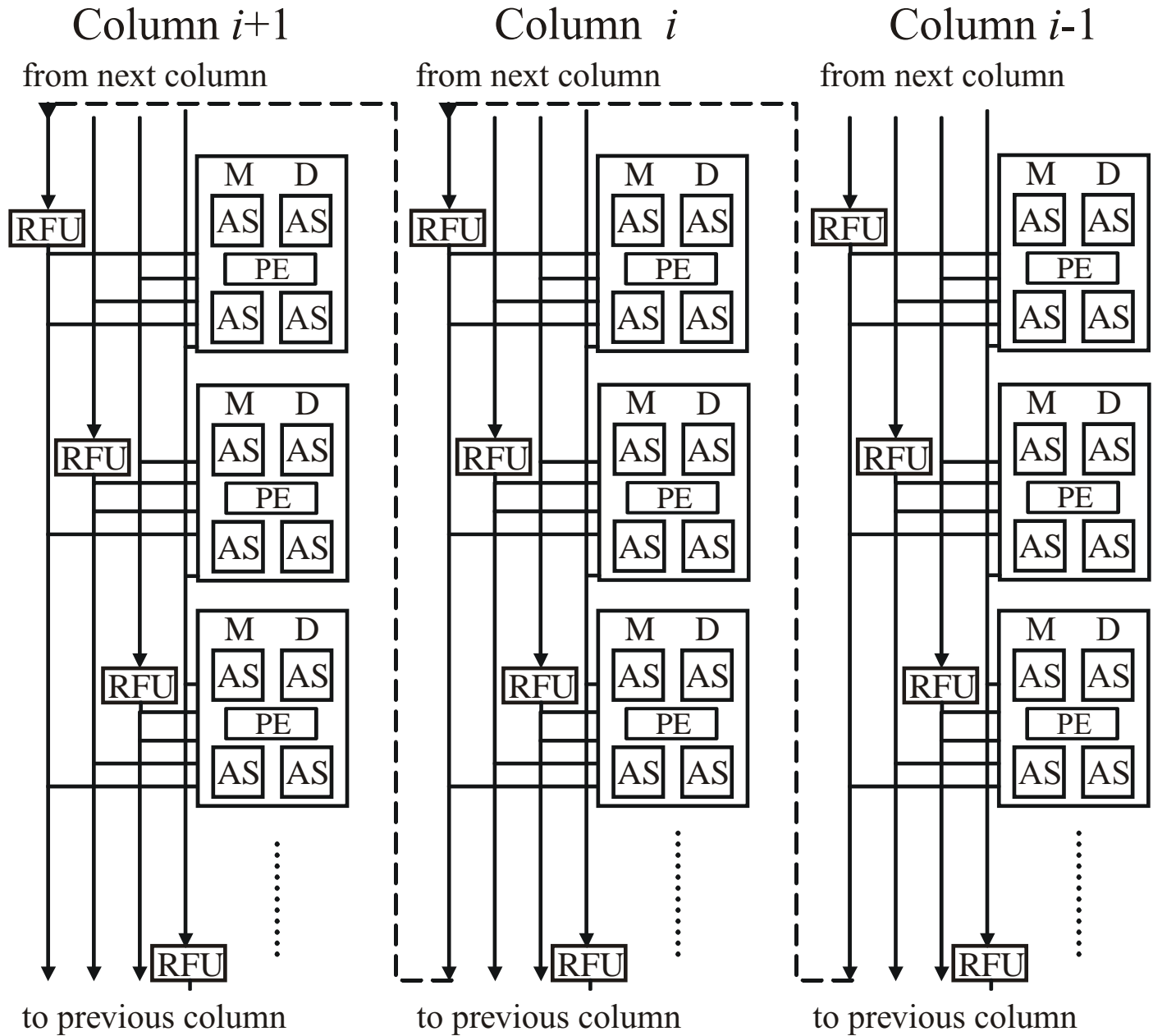
1 and **3** cannot (data dependency)

LEVO CPU Overview

- Uses modification of Tomasulo algorithm
 - (The original algorithm dates to 1964 and is used today in the Intel Pentium Pro, II, III & 4.)
- Instruction *time tags* enforce dependencies
- *Active Stations (AS)* hold instructions & data
- Communication buses segmented
 - → Short delay, high f
 - *Register Filter/Forwarding Units (RFUs)* link segments

LEVO

Archi-
tecture

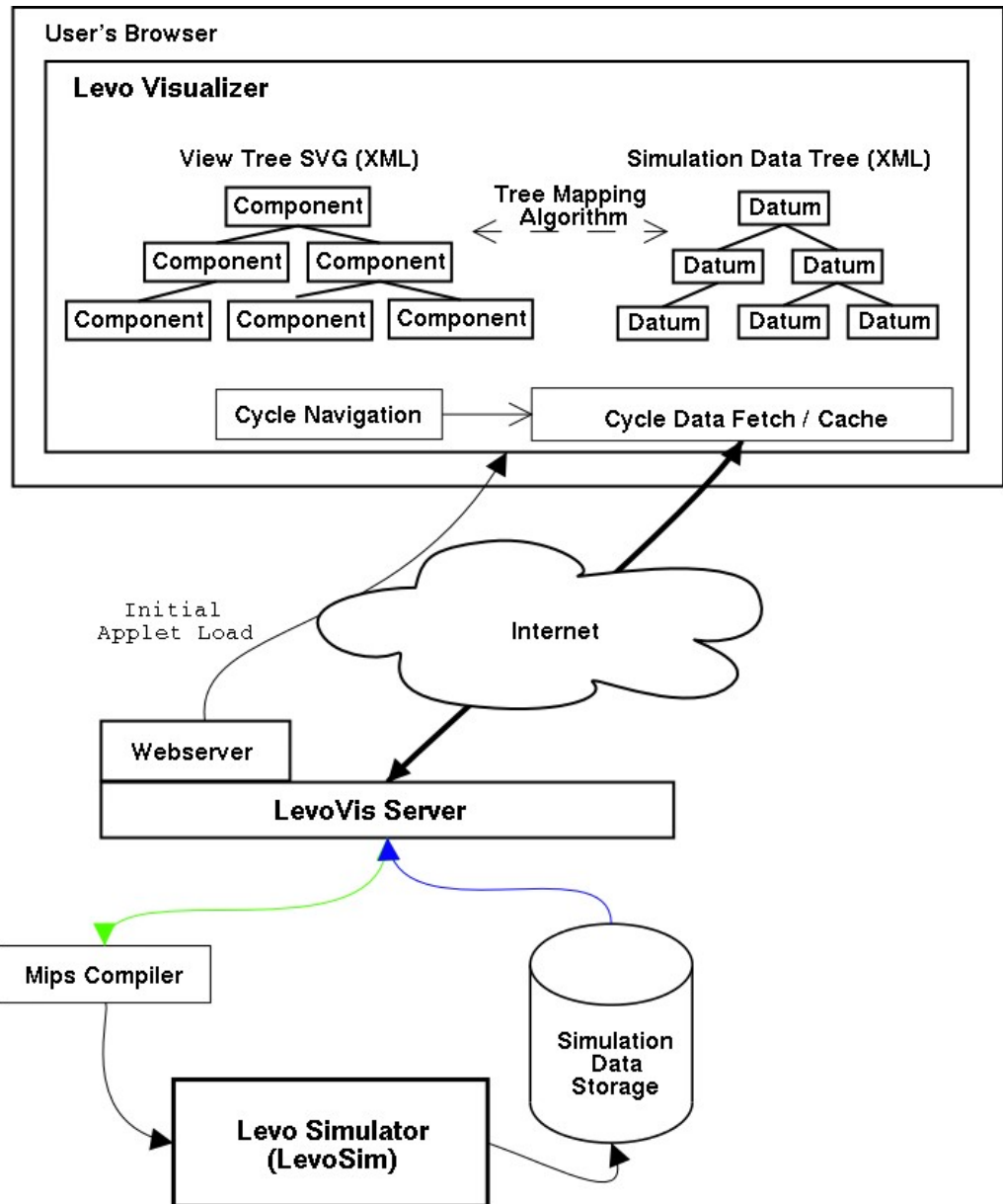


LEVOVIS Overview

- Based on XML and SVG
- SVG used to generate graphics
- XML links graphics with simulation data
- Simulation data files very large
 - → Kept on server
 - Data for individual cycles (10) brought over Web *as needed*
- *User able to navigate to arbitrary cycles*
- *Arbitrary display of machine elements*

LEVOVIS

Architecture



Data-to-Graphic Mapping Example

Simulation Data XML

<uid>

ffbe8d20

</uid>

SVG Graphic Component XML

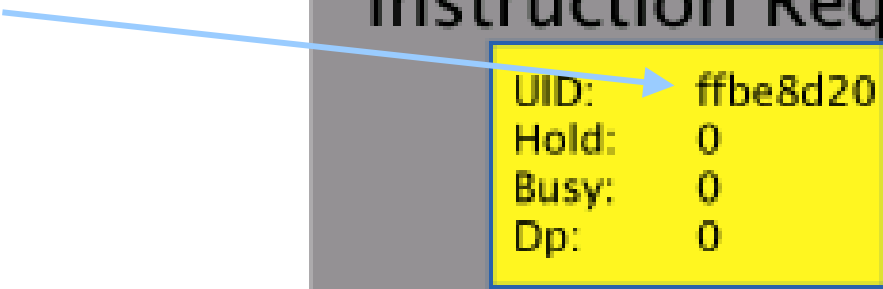
<g id="uid">

<tspan x="36" y="0">ffbe8d20</tspan>

</g>

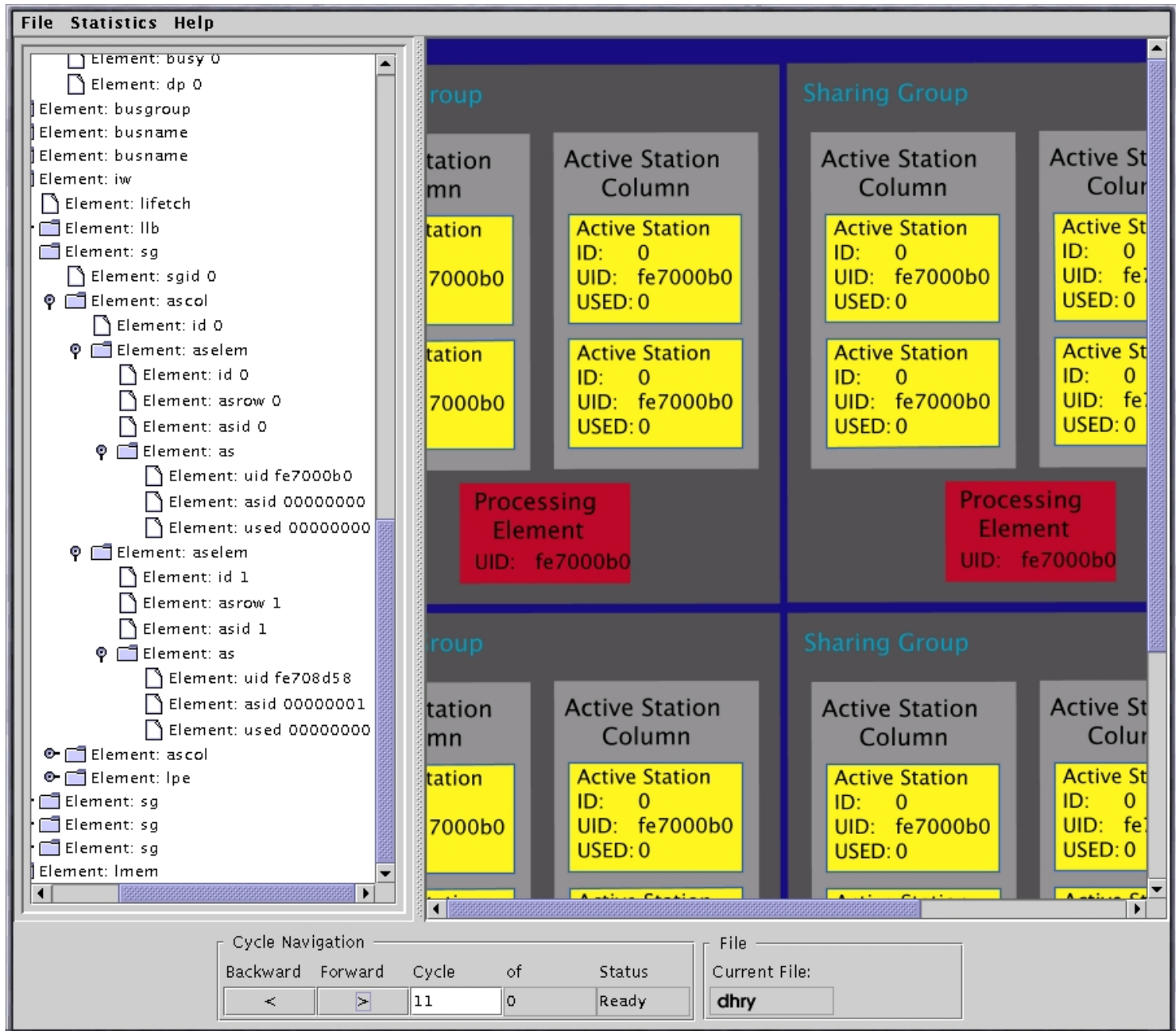
Gives

Instruction Request



UID:	ffbe8d20
Hold:	0
Busy:	0
Dp:	0

Levovis Example 1



Levovis Example 2

File Statistics Help

- Element: clock
 - Element: value 1
- Element: levo
 - Element: busgroup
 - Element: busgroup
 - Element: busgroup
 - Element: busname
 - Element: name instruction re
 - Element: rfbus
 - Element: busname
 - Element: name instruction re
 - Element: libus
 - Element: iw
 - Element: lifetch
 - Element: llb
 - Element: sg
 - Element: sg
 - Element: sgid 1
 - Element: ascol
 - Element: id 0
 - Element: aselem
 - Element: aselem
 - Element: ascol
 - Element: id 1
 - Element: aselem
 - Element: aselem
 - Element: lpe
 - Element: uid fe70002c
 - Element: sg
 - Element: sgid 2
 - Element: ascol
 - Element: ascol
 - Element: lpe

Instruction Window

Sharing Group 0

Active Station Column

Active Station

ID: 00000000
UID: fe7000b0
USED: 00000001
IA: 00400150
Inst: 8fa40000
dis: lw r4,0(r29)

Active Station Column

Active Station

ID: 00000004
UID: fe723350
USED: 00000000
IA: -
Inst: -
dis: -

Active Station

ID: 00000001
UID: fe708d58
USED: 00000001
IA: 00400154
Inst: 27a50004
dis: addiu r5,r29,4

Active Station

ID: 00000005
UID: fe72b0f8
USED: 00000000
IA: -
Inst: -
dis: -

Processing Element
UID: fe700000

Sharing Group 2

Active Station Column

Active Station

ID: 00000008
UID: fe7465f0
USED: 00000001
IA: 00400160
Inst: 00041080
dis: sll r2,r4,2

Active Station

ID: 0000000c
UID: fe769890
USED: 00000000
IA: -
Inst: -
dis: -

Active Station

ID: 00000009
UID: fe742998
USED: 00000001
IA: 00400164
Inst: 279c1a0
dis: addiu r28,r28,6896

Active Station

ID: 0000000d
UID: fe772538
USED: 00000001
IA: -
Inst: -
dis: -

Processing Element
UID: fe700058

Sharing Group 1

Active Station Column

Active Station

ID: 00000002
UID: fe711a00
USED: 00000001
IA: 00400158
Inst: 3c1c1001
dis: lui r28,0x1001

Active Station

ID: 00000006
UID: fe734ca0
USED: 00000000
IA: -
Inst: -
dis: -

Active Station

ID: 00000003
UID: fe71a0a8
USED: 00000001
IA: 0040015c
Inst: 24a60004
dis: addiu r6,r5,4

Active Station

ID: 00000007
UID: fe73c948
USED: 00000000
IA: -
Inst: -
dis: -

Processing Element
UID: fe70002c

Sharing Group 3

Active Station Column

Active Station

ID: 0000000a
UID: fe757f40
USED: 00000001
IA: 00400168
Inst: 00c23021
dis: addiu r6,r6,r2

Active Station

ID: 0000000e
UID: fe77b1e0
USED: 00000000
IA: -
Inst: -
dis: -

Active Station

ID: 0000000c
UID: fe760be8
USED: 00000001
IA: 0040016c
Inst: 3c011001
dis: lui r1,0x1001

Active Station

ID: 0000000f
UID: fe783e88
USED: 00000000
IA: -
Inst: -
dis: -

Processing Element
UID: fe700084

Memory Forwarding Bus

Cycle Navigation

Backward

Forward

Cycle

of

Status

<

>

12

4222

Ready

File

Current File:

dhry.xml

Online or Offline Demonstration

- ONLINE: Goto → WWW LevoVis
- OFFLINE: Goto → local LevoVis

Summary

- **LEVAVIS:**

- Many *flexible state visualization* capabilities
- Ideal for *complex CPU's*
- Usable for *any synchronous digital system*
- Gives *understanding, analysis* and *debugging* for researchers, students and engineers
- Allows *world-wide concurrent access* (Web-based)
- *Adaptable* to new systems or system requirements

Relevant Web Sites

Levo links:

www.ele.uri.edu/~uht

Or: www.levo.org

LevoVis direct:

ovel.ele.uri.edu:8080